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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application

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Title: ELECTRODE STRUCTURE AND METHOD FOR FORMING ELECTRODE STRUCTURE FOR A FLAT PANEL DISPLAY

The Commissioner of Patents and Trademarks
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Sir:

Transmittal of a Patent Application
(Under 37 CFR §1.53)

Transmitted herewith is the above identified patent application, including:

- ☒ Specification, claims and abstract, totaling 92 pages.
- ☐ Formal drawings, totaling _____ pages.
- ☒ Informal drawings, totaling 65 pages.
- ☒ Declaration and Power of Attorney.
- ☐ Information Disclosure statement.
- ☐ Form 1449
- ☐ Assignment(s)
- ☐ Assignment Recordation Form (duplicate)
- ☐ Preliminary Amendment

FEES DUE

The fees due for filing the specification pursuant to 37 C.F.R. § 1.16 and for recording of the Assignment, if any, are determined as follows:

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					\$760.00
Total Claims	69	Minus 20=	49	X \$18 =	\$882.00
Independent Claims	8	Minus 3=	5	X \$78=	\$390.00
If multiple dependent claims are presented, add \$260.00					\$0.00
Add Assignment Recording Fee of \$40.00 If Assignment document is enclosed					\$0.00
TOTAL APPLICATION FEE DUE					\$2,032.00

PAYMENT OF FEES

The full fee due in connection with this communication is provided as follows:

1. Not enclosed
 - ☐ No filing fee is to be paid at this time.
2. Enclosed
 - ☒ Filing fee
 - ☐ Recording assignment
 - ☐ Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached
 - ☐ For processing an application with specification in a non-English language
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 - ☒ The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.
 - ☒ A check in the amount of \$2,032.00
 - ☐ Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

This application is filed pursuant to 37 C.F.R. § 1.53 in the name of the above-identified Inventor(s).

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- ☒ This transmittal ends with this page.

Respectfully submitted,

Date:

10/19/99

By:


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UNITED STATES PATENT APPLICATION

FOR

ELECTRODE STRUCTURE AND METHOD FOR FORMING ELECTRODE
STRUCTURE FOR A FLAT PANEL DISPLAY

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ELECTRODE STRUCTURE AND METHOD FOR FORMING ELECTRODE
STRUCTURE FOR A FLAT PANEL DISPLAY

FIELD OF THE INVENTION

The present claimed invention relates to the field of flat panel displays. More particularly, the present
5 claimed invention relates to a method for forming an electrode structure for a flat panel display.

BACKGROUND ART

Display devices such as, for example, flat panel
10 display devices typically utilize a cathode structure that is formed over a backplate. The cathode structure includes row electrodes and column electrodes that are used to activate regions of field emitters. The field emitters emit electrons that are directed towards
15 respective pixel or sub-pixel regions on a faceplate. By selectively activating row electrodes and column electrodes, electrons are emitted that strike the respective pixel or sub-pixel regions on the faceplate. Typically, phosphors are coated on the inside of the
20 faceplate. The electrons strike the phosphors, producing red, green or blue visible light that forms a visible display.

In prior art processing techniques, aluminum is commonly used for forming row electrodes and column electrodes. However, aluminum is subject to hillock formation. Hillock formation results in nonuniform
5 planarization and can cause both row and column shorts to occur.

In one recent prior art process a layer of tantalum is deposited over the aluminum layer for reducing hillock
10 formation. However, the resulting structure has a conductivity that is too low for use in large flat panel display devices. That is, though this process is sufficient for making small flat panel displays, the resulting row or column has too high a resistivity to be
15 used in making large flat panel displays.

In prior art processes that use a layer of aluminum that is overlain by a layer of tantalum, the layer of aluminum is first deposited by placing the backplate into
20 a sputtering chamber. Once the aluminum layer deposition is complete, the backplate is removed from the sputtering chamber. The layer of aluminum is then masked. More particularly, photoresist is deposited over the backplate, and the photoresist is exposed. The layer of aluminum is

then etched using a wet etch process to form the desired aluminum structure.

5 The backplate is then placed into a second sputtering chamber that deposits the tantalum layer. Once the deposition of the tantalum layer is complete, the backplate is removed from the second sputtering chamber. The layer of tantalum is then masked. More particularly, photoresist is deposited over the backplate, and the
10 photoresist is exposed. The tantalum layer is then etched. Because wet etch processes are not effective for etching tantalum, prior art processes must use a dry etch process. In one recent prior art process a reactive ion etch is used for etching the tantalum layer.

15

The use of two separate sputtering deposition steps is expensive and time consuming. Also, the use of two separate masking process steps is expensive and time consuming. These factors result in a low manufacturing
20 yield and throughput. In addition, the steepness of the row electrodes and column electrodes of prior art processes results in manufacturing defects related to cracking of the overlying tantalum layer.

The dry etch process is complex. Also, the use of a dry etch process is expensive as it requires the use of expensive capital equipment (e.g. reactive ion etcher). Moreover, the dry etch process is corrosive to aluminum and can result in corrosion of the aluminum layer when pinholes are present in the tantalum layer. In addition, the dry etch process forms polymers within the tantalum layer. Thus, following the dry etch, a polymer strip process is required for removing the polymers. The polymer strip process is expensive. In addition, the corrosive dry etch process can result in pinholes in the glass backplate.

During subsequent conventional process steps, the column electrode is subjected to potential damage. More particularly damage often results from, ion bombardment, cavity etch, cone deposition, dielectric deposition, masking and etching of the dielectric layer, deposition and etch of a molybdenum layer, deposition and etch of a chromium layer, polyimide deposition, etc. These process steps lead to shorts and opens that result in reduced yield and device failure.

Another problem that occurs in prior art devices is column to focus waffle shorts. These column to focus waffle shorts lead to reduced yield and device failure. In addition, the electrodes used in prior art column
5 electrodes can react with the frit seal in the frit seal region, leading to shorts between column electrodes.

Thus, a need exists for an electrode structure and a method for forming an electrode structure that does not
10 result in hillock formation. Still another need exists for an electrode structure and a method for forming an electrode structure that meets the above-listed needs but which does not produce undesired electrical shorts or opens in the cathode structure. Still another need exists
15 for an electrode structure and a method for forming an electrode structure that meets the above-listed needs and that is inexpensive to manufacture and that does not result in reduced yield.

SUMMARY OF INVENTION

The present invention provides an electrode structure and a method for forming an electrode structure that does not result in hillock formation. Also, the present
5 invention provides an electrode structure and a method for forming an electrode structure that meets the above-listed need but which does not produce undesired electrical shorts or opens in the cathode structure. Also, the present invention provides an electrode structure and a
10 method for forming an electrode structure that meets the above-listed needs and that is inexpensive and that increases yield and throughput.

In one embodiment of the present invention, an
15 electrode structure for a flat panel display is shown that includes lower electrodes and upper electrodes. In the present embodiment, the lower electrodes are row electrodes and the upper electrodes are column electrodes. The lower electrodes and the upper electrodes are
20 separated by a resistive layer and a dielectric layer. In one embodiment, both the upper electrodes and the lower electrodes are formed of a metal alloy. In one embodiment, the metal alloy is an aluminum alloy. Alternatively, a silver alloy is used.

25

A method for forming an electrode structure of a flat panel display is disclosed. First, a metal alloy layer is deposited over a backplate. A cladding layer is then deposited over the metal alloy layer. A wet etch step is then performed so as to form a layer of electrodes. By performing the deposition of the metal alloy layer and the cladding layer in the same sputtering tool sequentially, cost savings, increased yield and throughput result as compared to prior art processes that require two separate trips to a sputtering tool. Moreover, because a single masking step and a single wet etch is required, significant cost savings, increased yield and throughput result as compared to prior art processes that require two separate masking steps and etch steps.

The present invention does not use a dry etch process. Thus, significant cost savings are realized because there is no need for complex and expensive capital equipment for performing the dry etch process. In addition, because the present invention does not use a dry etch process, there is no corrosion of an underlying aluminum layer and no damage (e.g. pinholes) to the glass backplate. Moreover, because the present invention does not use a dry etch process, there is no need to perform a polymer strip process. This results in further time and

cost savings as compared to prior art processes and increased throughput and yield.

In one embodiment, a passivation layer is deposited
5 over the upper electrode. In the present embodiment, the passivation layer is silicon nitride. The silicon nitride layer is then masked and etched. The resulting silicon nitride structure partially covers the upper electrodes. This protects the upper electrodes during subsequent
10 process steps.

Gate metal is then deposited, masked and etched to form a gate structure. The passivation layer protects the upper electrodes during deposition, mask and etch
15 steps. Conventional process steps are then used to complete the cathode structure. In one embodiment of the present conventional process steps are used to form emitters and to form a focusing structure. In the present embodiment, these process steps include ion bombardment,
20 cavity etch, cone deposition, dielectric deposition, masking and etching of the dielectric layer, deposition and etch of molybdenum layer, deposition and etch of chromium layer, polyimide deposition, etc. During these process steps, the upper electrodes are protected by the
25 passivation layer. Thus, damage to upper electrodes is

prevented. By preventing damage to upper electrodes, column shorts and opens are reduced. Also, because there is less exposed metal alloy, column to focus waffle shorts are decreased.

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The use of either an aluminum alloy or the use of a silver alloy provides good conductivity. The resulting conductivity is sufficient for fabrication of large flat panel displays. In addition, the present invention
10 prevents hillock formation as occurs in prior art processes that use aluminum. Thus, electrical shorts and opens are prevented as compared with prior art processes that use aluminum and good planarity of overlying layers is obtained. This results in increased yield as compared
15 with prior art processes that use aluminum.

Thus, the present invention provides an electrode structure and a method for forming an electrode structure that does not result in hillock formation. Also, the
20 present invention provides an electrode structure and a method for forming an electrode structure that meets the above-listed need but which does not produce undesired electrical shorts or opens in the cathode structure. Also, the present invention provides an electrode structure and
25 a method for forming an electrode structure that meets the

above-listed needs, that is inexpensive and that increases yield and throughput.

These and other objects and advantages of the present
5 invention will no doubt become obvious to those of
ordinary skill in the art after having read the following
detailed description of the preferred embodiments which
are illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrates embodiments of the invention and, together with the
5 description, serve to explain the principles of the invention:

FIGURE 1 is a diagram showing a method for forming an electrode structure of a display device in accordance with
10 one embodiment of the present invention.

FIGURE 2 is a side sectional view of a display device showing a backplate over which a metal alloy layer is deposited in accordance with one embodiment of the present
15 invention.

FIGURE 3 is a side sectional view of a display device showing the deposition of a cladding layer in accordance with one embodiment of the present invention.
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FIGURE 4A is a side sectional view of a display device showing an expanded view of the structure of Figure 3 after mask and etch steps have formed a lower electrode in accordance with one embodiment of the present claimed
25 invention.

FIGURE 4B is a side sectional view of a display device showing an expanded view of the structure of Figure 3 after mask and etch steps have formed a lower electrode in accordance with one embodiment of the present claimed invention.

FIGURE 5A is a side sectional view of a display device showing the structure of Figure 4A after the deposition of a resistor layer in accordance with one embodiment of the present claimed invention.

FIGURE 5B is a side sectional view of a display device showing the structure of Figure 4B after the deposition of a resistor layer in accordance with one embodiment of the present claimed invention.

FIGURE 6A is a side sectional view of a display device showing the structure of Figure 5A after the deposition of a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 6B is a side sectional view of a display device showing the structure of Figure 5B after the deposition of a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 7A is a side sectional view of a display device showing the structure of Figure 6A after the deposition of a metal alloy layer in accordance with one
5 embodiment of the present claimed invention.

FIGURE 7B is a side sectional view of a display device showing the structure of Figure 6B after the deposition of a metal alloy layer in accordance with one
10 embodiment of the present claimed invention.

FIGURE 8A is a side sectional view of a display device showing the structure of Figure 7A after the deposition of a cladding layer in accordance with one
15 embodiment of the present claimed invention.

FIGURE 8B is a side sectional view of a display device showing the structure of Figure 7B after the deposition of a cladding layer in accordance with one
20 embodiment of the present claimed invention.

FIGURE 9A is a side sectional view of a display device showing the structure of Figure 8A after mask and etch steps have been performed in accordance with one
25 embodiment of the present claimed invention.

FIGURE 9B is a side sectional view of a display device showing the structure of Figure 8B after mask and etch steps have been performed in accordance with one
5 embodiment of the present claimed invention.

FIGURE 10A is a side sectional view of a display device showing the structure of Figure 9A after the deposition of a passivation layer in accordance with one
10 embodiment of the present claimed invention.

FIGURE 10B is a side sectional view of a display device showing the structure of Figure 9B after the deposition of a passivation layer in accordance with one
15 embodiment of the present claimed invention.

FIGURE 11A is a side sectional view of a display device showing the structure of Figure 10A after mask and etch steps have been performed in accordance with one
20 embodiment of the present claimed invention.

FIGURE 11B is a side sectional view of a display device showing the structure of Figure 10B after mask and etch steps have been performed in accordance with one
25 embodiment of the present claimed invention.

FIGURE 12A is a side sectional view of a display device showing the structure of Figure 11A after deposition of a gate metal layer in accordance with one
5 embodiment of the present claimed invention.

FIGURE 12B is a side sectional view of a display device showing the structure of Figure 11B after deposition of a gate metal layer in accordance with one
10 embodiment of the present claimed invention.

FIGURE 13A is a side sectional view of a display device showing the structure of Figure 12A after mask and etch steps have been performed in accordance with one
15 embodiment of the present claimed invention.

FIGURE 13B is a side sectional view of a display device showing the structure of Figure 12B after mask and etch steps have been performed in accordance with one
20 embodiment of the present claimed invention.

FIGURE 14A is a side sectional view of a display device showing the structure of Figure 13A after formation of emitters and focus structure in accordance with one
25 embodiment of the present claimed invention.

FIGURE 14B is a side sectional view of a display device showing the structure of Figure 13B after formation of emitters and focus structure in accordance with one
5 embodiment of the present claimed invention.

FIGURE 15 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.
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FIGURE 16A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate structure in accordance with
15 one embodiment of the present claimed invention.

FIGURE 16B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a
20 dielectric layer, and a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 16C is a side sectional view of a display device showing the structure of Figure 9A after
25 deposition, mask and etch have formed a passivation layer

in accordance with one embodiment of the present claimed invention.

FIGURE 16D is a side sectional view of a display device showing the structure of Figure 9B after deposition, mask and etch have formed a passivation layer in accordance with one embodiment of the present claimed invention.

FIGURE 16E is a side sectional view of a display device showing the structure of Figure 16C after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 16F is a side sectional view of a display device showing the structure of Figure 16D after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 16G is a side sectional view of a display device showing the structure of Figure 16E after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 16H is a side sectional view of a display device showing the structure of Figure 16F after evaporation of a chromium layer and deposition of cone
5 material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 16I is a side sectional view of a display
10 device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

FIGURE 16J is a side sectional view of a display device showing a completed cathode structure in accordance
15 with one embodiment of the present claimed invention.

FIGURE 17 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.
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FIGURE 18A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate layer in accordance with one
25 embodiment of the present claimed invention.

FIGURE 18B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a
5 dielectric layer, and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 18C is a side sectional view of a display device showing the structure of Figure 18A after mask and
10 etch steps have formed a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 18D is a side sectional view of a display device showing the structure of Figure 18B after mask and
15 etch steps have formed a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 18E is a side sectional view of a display device showing the structure of Figure 18C after mask and
20 etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18F is a side sectional view of a display device showing the structure of Figure 18D after mask and

etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18G is a side sectional view of a display device showing the structure of Figure 18E after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18H is a side sectional view of a display device showing the structure of Figure 18F after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18I is a side sectional view of a display device showing the structure of Figure 18G after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 18J is a side sectional view of a display device showing the structure of Figure 18H after evaporation of a chromium layer and deposition of cone

material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

5 FIGURE 18K is a side sectional view of a display device showing the structure of Figure 18I after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

10 FIGURE 18L is a side sectional view of a display device showing the structure of Figure 18J after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

15 FIGURE 18M is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

20 FIGURE 18N is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

25 FIGURE 19 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 20A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, a tantalum layer, and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 20B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, a tantalum layer and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 20C is a side sectional view of a display device showing the structure of Figure 20A after mask and etch steps have formed a tantalum structure and a gate structure in accordance with one embodiment of the present claimed invention.

FIGURE 20D is a side sectional view of a display device showing the structure of Figure 20B after mask and etch steps have formed a tantalum structure and a gate

structure in accordance with one embodiment of the present claimed invention.

FIGURE 20E is a side sectional view of a display device showing the structure of Figure 20C after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 20F is a side sectional view of a display device showing the structure of Figure 20D after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 20G is a side sectional view of a display device showing the structure of Figure 20E after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 20H is a side sectional view of a display device showing the structure of Figure 20F after evaporation of a chromium layer and deposition of cone

material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

5 FIGURE 20I is a side sectional view of a display device showing the structure of Figure 20G after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

10 FIGURE 20J is a side sectional view of a display device showing the structure of Figure 20H after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

15 FIGURE 20K is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

20 FIGURE 20L is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

25 FIGURE 21 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 22A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate layer in accordance with one
5 embodiment of the present claimed invention.

FIGURE 22B is a side sectional view of a display device showing a backplate over which lower and upper
10 electrodes are formed and having a resistor layer, a dielectric layer, and a gate layer in accordance with one embodiment of the present claimed invention.

FIGURE 22C is a side sectional view of a display device showing the structure of Figure 22A after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one
15 embodiment of the present claimed invention.

FIGURE 22D is a side sectional view of a display device showing the structure of Figure 22B after the deposition of a passivation layer and after mask and etch steps have been performed in accordance with one
20 embodiment of the present claimed invention.

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FIGURE 22E is a side sectional view of a display device showing the structure of Figure 22C after the deposition, mask and etch of a dielectric layer in accordance with one embodiment of the present claimed
5 invention.

FIGURE 22F is a side sectional view of a display device showing the structure of Figure 22D after the deposition, mask and etch of a dielectric layer in
10 accordance with one embodiment of the present claimed invention.

FIGURE 22G is a side sectional view of a display device showing the structure of Figure 22E after an etch
15 step has been performed so as to form a cavity in accordance with one embodiment of the present claimed invention.

FIGURE 22H is a side sectional view of a display
20 device showing the structure of Figure 22F after an etch step has been performed so as to form a cavity in accordance with one embodiment of the present claimed invention.

FIGURE 22I is a side sectional view of a display device showing the structure of Figure 22G after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22J is a side sectional view of a display device showing the structure of Figure 22H after evaporation of a chromium layer and deposition of cone material, deposition of a layer of dielectric material, and mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22K is a side sectional view of a display device showing the structure of Figure 22I after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22L is a side sectional view of a display device showing the structure of Figure 22J after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 22M is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

5 FIGURE 22N is a side sectional view of a display device showing a completed cathode structure in accordance with one embodiment of the present claimed invention.

10 FIGURE 23 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

15 FIGURE 24A is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate structure in accordance with one embodiment of the present claimed invention.

20 FIGURE 24B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a dielectric layer, and a gate structure in accordance with one embodiment of the present claimed invention.

25

FIGURE 24C is a side sectional view of a display device showing the structure of Figure 24A after deposition of a sputtered molybdenum layer, deposition of an evaporated molybdenum layer, and deposition of a sputtered molybdenum layer in accordance with one embodiment of the present claimed invention.

FIGURE 24D is a side sectional view of a display device showing the structure of Figure 24B after deposition of a sputtered molybdenum layer, deposition of an evaporated molybdenum layer, and deposition of a sputtered molybdenum layer in accordance with one embodiment of the present claimed invention.

FIGURE 24E is a side sectional view of a display device showing the structure of Figure 24C after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24F is a side sectional view of a display device showing the structure of Figure 24D after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24G is a side sectional view of a display device showing the structure of Figure 24E after deposition of a dielectric layer and a passivation layer in accordance with one embodiment of the present claimed
5 invention.

FIGURE 24H is a side sectional view of a display device showing the structure of Figure 24F after deposition of a dielectric layer and a passivation layer
10 in accordance with one embodiment of the present claimed invention.

FIGURE 24I is a side sectional view of a display device showing the structure of Figure 24G after mask and
15 etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24J is a side sectional view of a display device showing the structure of Figure 24H after mask and
20 etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24K is a side sectional view of a display device showing the structure of Figure 24I after mask and
25 etch steps have been performed and after focusing

structures have been formed in accordance with one embodiment of the present claimed invention.

FIGURE 24L is a side sectional view of a display device showing the structure of Figure 24J after mask and etch steps have been performed and after focusing structures have been formed in accordance with one embodiment of the present claimed invention.

FIGURE 24M is a side sectional view of a display device showing the structure of Figure 24K after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 24N is a side sectional view of a display device showing the structure of Figure 24L after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 25 is a diagram showing a method for forming an electrode structure of a display device in accordance with one embodiment of the present invention.

FIGURE 26A is a side sectional view of a display device showing a backplate over which lower and upper

electrodes are formed and having a resistor layer, a dielectric layer, a gate structure, a sputtered molybdenum layer, an evaporated molybdenum layer, and a sputtered molybdenum layer, after mask and etch steps and after the
5 deposition of a dielectric layer in accordance with one embodiment of the present claimed invention.

FIGURE 26B is a side sectional view of a display device showing a backplate over which lower and upper
10 electrodes are formed and having a resistor layer, a dielectric layer, a gate structure, a sputtered molybdenum layer, an evaporated molybdenum layer, and a sputtered molybdenum layer, after mask and etch steps and after the deposition of a dielectric layer in accordance with one
15 embodiment of the present claimed invention.

FIGURE 26C is a side sectional view of a display device showing the structure of Figure 26A after mask and etch steps have been performed in accordance with one
20 embodiment of the present claimed invention.

FIGURE 26D is a side sectional view of a display device showing the structure of Figure 26B after mask and etch steps have been performed in accordance with one
25 embodiment of the present claimed invention.

FIGURE 26E is a side sectional view of a display device showing the structure of Figure 26C after mask and etch steps have been performed in accordance with one
5 embodiment of the present claimed invention.

FIGURE 26F is a side sectional view of a display device showing the structure of Figure 26D after mask and etch steps have been performed in accordance with one
10 embodiment of the present claimed invention.

FIGURE 26G is a side sectional view of a display device showing the structure of Figure 26E after mask and etch steps have been performed in accordance with one
15 embodiment of the present claimed invention.

FIGURE 26H is a side sectional view of a display device showing the structure of Figure 26F after mask and etch steps have been performed in accordance with one
20 embodiment of the present claimed invention.

FIGURE 26I is a side sectional view of a display device showing the structure of Figure 26G after mask and etch steps and formation of a focusing structure in

accordance with one embodiment of the present claimed invention.

FIGURE 26J is a side sectional view of a display
5 device showing the structure of Figure 26H after mask and
etch steps and formation of a focusing structure in
accordance with one embodiment of the present claimed
invention.

10 FIGURE 26K is a side sectional view of a display
device showing the structure of Figure 26I after mask and
etch steps have been performed in accordance with one
embodiment of the present claimed invention.

15 FIGURE 26L is a side sectional view of a display
device showing the structure of Figure 26J after mask and
etch steps have been performed in accordance with one
embodiment of the present claimed invention.

20 FIGURE 27 is a diagram showing a method for forming
an electrode structure of a display device in accordance
with one embodiment of the present invention.

FIGURE 28A is a side sectional view of a display
25 device showing a backplate over which lower and upper

electrodes are formed and having a resistor layer, a dielectric layer, a gate structure, an evaporated chromium layer, an evaporated molybdenum layer, and a dielectric layer in accordance with one embodiment of the present
5 claimed invention.

FIGURE 28B is a side sectional view of a display device showing a backplate over which lower and upper electrodes are formed and having a resistor layer, a
10 dielectric layer, a gate structure, an evaporated chromium layer, an evaporated molybdenum layer, and a dielectric layer in accordance with one embodiment of the present claimed invention.

15 FIGURE 28C is a side sectional view of a display device showing the structure of Figure 28A after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

20 FIGURE 28D is a side sectional view of a display device showing the structure of Figure 28B after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

FIGURE 28E is a side sectional view of a display device showing the structure of Figure 28C after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

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FIGURE 28F is a side sectional view of a display device showing the structure of Figure 28D after mask and etch steps have been performed in accordance with one embodiment of the present claimed invention.

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FIGURE 28G is a side sectional view of a display device showing the structure of Figure 28E after focusing structures have been formed in accordance with one embodiment of the present claimed invention.

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FIGURE 28H is a side sectional view of a display device showing the structure of Figure 28F focusing structures have been formed in accordance with one embodiment of the present claimed invention.

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FIGURE 28I is a side sectional view of a display device showing the structure of Figure 28G after an etch step has been performed in accordance with one embodiment of the present claimed invention.

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FIGURE 28J is a side sectional view of a display device showing the structure of Figure 28H after an etch step has been performed in accordance with one embodiment of the present claimed invention.

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FIGURE 28K is a side sectional view of a display device showing the structure of Figure 28I after an etch step has been performed in accordance with one embodiment of the present claimed invention.

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FIGURE 28L is a side sectional view of a display device showing the structure of Figure 26J after an etch step has been performed in accordance with one embodiment of the present claimed invention.

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The drawings referred to in this description should be understood as not being drawn to scale except if specifically noted.

20

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention.

However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

With reference now to Figure 1, a method for forming an electrode structure for a display device is shown. As shown by step 101, a metal alloy layer is deposited.

Figure 2 shows a metal alloy layer 2 deposited over glass plate 1.

In one embodiment, metal alloy layer 2 is an aluminum alloy. In one embodiment, metal alloy layer 2 has a thickness of 500-5000 Angstroms. In one specific embodiment, an aluminum alloy is used that includes aluminum (Al) and Neodymium (Nd). In the present embodiment, the aluminum alloy has an concentration of from .5 to 6 atomic percent Nd. In another embodiment, an aluminum alloy is used that has a concentration of from .5 to 6 atomic percent Nd and from 0 to 5 atomic percent titanium (Ti).

Continuing with Figures 1-2, in an alternate embodiment, metal alloy layer 2 is a silver alloy. In one embodiment a silver alloy is used that includes silver (Ag) and .5 to 2 atomic percent palladium (Pd) and .5 to 2 atomic percent copper (Cu). In yet another embodiment, a silver alloy is used that includes .5 percent to 2 atomic percent palladium and 0.0 to 2.0 atomic percent titanium.

When a silver alloy is used, an adhesion layer can be used to promote adhesion to the glass plate. In one

embodiment, a molybdenum adhesion layer is used that has a thickness of approximately 500-1000 angstroms.

Referring to Figure 1, as shown by step 102, a
5 cladding layer is then deposited. Figure 3 shows the structure of Figure 2 after cladding layer 3 has been deposited. It can be seen that cladding layer 3 directly overlies metal alloy layer 2.

10 In one embodiment, cladding layer 3 of Figure 3 is a molybdenum (Mo) tungsten (W) alloy. In the present embodiment, cladding layer 3 has a thickness of approximately 500-4000 angstroms. The use of cladding layer 3 produces a contact pad that is reliable and that
15 maintains good electrical contact. In addition, the use of cladding layer 3 further reduces hillock formation.

Though the present invention includes the deposition of cladding layer 3, the present invention is well adapted
20 for use without cladding layer 3. That is, the use of aluminum alloy or silver alloy provides sufficient reduction in hillock formation and results in good conductivity as compared with prior art processes.

In one embodiment, a diffusion barrier layer is used. The diffusion barrier layer can be formed of is titanium, titanium nitride or titanium tungsten that is deposited directly over the silver alloy. In one embodiment, a
5 diffusion barrier layer is used that has a thickness of approximately 500-2000 Angstroms. The use of a diffusion barrier layer is particularly useful in an embodiment that does not include a cladding layer.

10 In one embodiment, the deposition of metal alloy layer 2 and cladding layer 3 is conducted using a single sputtering tool. That is, in the present invention, a sputtering process is used whereby metal alloy layer 2 and cladding layer 3 are sequentially deposited in a single
15 sputtering tool. More particularly, in one embodiment, glass plate 1 is placed into a sputtering tool that includes a sputtering chamber that first deposits metal alloy layer 2 and then deposits cladding layer 3. The glass plate is then removed from the sputtering chamber.
20 This provides significant cost savings over prior art methods that require two separate sputtering process steps and results in increased throughput and yield.

The use of either an aluminum alloy or the use of a
25 silver alloy in conjunction with a cladding layer provides

good conductivity. The resulting conductivity is sufficient for fabrication of large flat panel displays. In addition, the present invention prevents hillock formation as occurs in prior art processes that use aluminum. Thus, shorts are prevented as compared with prior art processes that use aluminum and planarity of overlying layers is obtained. This results in increased yield as compared with prior art processes that use aluminum.

10

Referring back to Figure 1, mask and etch steps are performed as shown by step 103. More particularly, in the present embodiment, photoresist is deposited over the backplate and is patterned. The backplate is then etched using a wet etch process to form the desired row electrodes. Figures 4A-4B show the structure of Figure 3 after mask and etch steps have formed exemplary lower electrode 4.

15

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The present invention requires a single patterning step and a single etch step in order to form row electrodes. Thus, the present invention does not require two separate patterning steps as are required in prior art processes. This results in significant cost savings as compared to prior art processes that require two separate

25

patterning steps. In addition, because the present invention does not require two separate etch steps as are required in prior art processes that use a molybdenum cap, the present invention results in increased yield and
5 throughput.

The present invention does not use a dry etch process for forming row electrodes. Thus, significant cost savings are realized because there is no need for complex
10 and expensive capital equipment for performing the dry etch process. In addition, because the present invention does not use a dry etch process, there is no corrosion of an underlying aluminum layer and no damage (e.g. pinholes) to the glass backplate. Moreover, because the present
15 invention does not use a dry etch process, there is no need to perform a polymer strip process. This results in further increases in throughput and yield as compared to prior art processes.

20 In one embodiment, the etching process forms angled edges. In the present embodiment, an etchant is used that includes nitric acid, phosphoric acid, ascectic acid and water. The use of this etchant performs a controlled lifting of the photoresist and results in angled edges on
25 the sides of the lower electrode 4. The use of angled

edges results in good conformity of overlying layers and reduces cracking in overlying layers.

Referring back to Figure 1, a resistor layer is
5 deposited as shown by step 104. In the embodiment shown
in Figures 5A-5B, resistor layer 5 is shown to overlie
lower electrode 4. In one embodiment, resistor layer 5
has a thickness of approximately 2000 angstroms. In the
present embodiment, resistor layer 5 is silicon carbide
10 (SiC) that is either deposited using a sputtering process
or a chemical vapor deposition process.

A layer of dielectric is then deposited as shown by
step 105 of Figure 1. In one embodiment silicon dioxide
15 (SiO₂) is used as a dielectric. In the present embodiment,
a plasma enhanced chemical vapor deposition process is
used to deposit the silicon dioxide layer. Referring now
to Figures 6A-6B, the embodiment of Figures 5A-5B is shown
after the deposit of dielectric layer 6.

20

A metal alloy layer is then deposited as shown by
step 106 of Figure 1. In the present embodiment, the
metal alloy layer has a thickness of approximately 500-
5000 Angstroms. Figures 7A-7B show metal alloy layer 11
25 deposited over dielectric layer 6. In one embodiment,

metal alloy layer 11 is an aluminum alloy. More particularly, in one specific embodiment, an aluminum alloy is used that includes aluminum and from .5 to 6 atomic percent neodymium and from 0 to 5 atomic percent titanium.

Alternatively, metal alloy layer 11 is a silver alloy. In one embodiment, metal alloy layer 11 includes silver and .5 to 2 atomic percent palladium and .5 to 2 atomic percent copper. In yet another embodiment, a silver alloy is used that includes .5 percent to 2 atomic percent palladium Pd and 0.0 to 2.0 atomic percent titanium.

When a silver alloy is used an adhesion layer can be used to promote adhesion to the gate structure. In one embodiment, a molybdenum adhesion layer is used that has a thickness of approximately 500-1000 angstroms is used.

Referring to Figure 1, as shown by step 107, a cladding layer is then deposited. Figure 8A-8B shows the structure of Figures 7A-7B after cladding layer 12 has been deposited. It can be seen that cladding layer 12 directly overlies metal alloy layer 11.

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In one embodiment, cladding layer 12 of Figure 3 is a molybdenum tungsten alloy. In the present embodiment, cladding layer 12 has a thickness of approximately 500 - 4000 angstroms. The use of cladding layer 12 produces a
5 contact pad that is reliable and that maintains good electrical contact. In addition, the use of cladding layer 12 further reduces hillock formation.

Though the present invention includes the deposition
10 of cladding layer 12, the present invention is well adapted for use without cladding layer 12. That is, the use of aluminum alloy or silver alloy provides sufficient reduction in hillock formation and results in good conductivity as compared with prior art processes. In an
15 embodiment that does not include cladding layer 12 but which uses a silver alloy, a diffusion barrier layer can be used. In one embodiment, the diffusion barrier layer is titanium or titanium nitride or titanium tungsten that is deposited over the silver alloy and that has a
20 thickness of approximately 500-2000 Angstroms.

In one embodiment, the deposition of metal alloy layer 11 and cladding layer 12 is conducted using a single sputtering tool. This provides significant cost savings
25 over prior art methods that require two separate

sputtering process steps and results in increased throughput and yield.

Referring to step 108 of Figure 1, mask and etch steps are performed for forming upper electrodes. In the present invention, a wet etch process is used. Figure 9A-9B show the structure of Figures 8A-8B after mask and etch steps have formed exemplary upper electrode 14. In one embodiment, an etchant is used that includes nitric acid, phosphoric acid, ascorbic acid and water for forming angled edges on the sides of upper electrode 14. The use of an angled edges results in good conformity of overlying layers and reduces cracking in overlying layers.

The use of either an aluminum alloy or the use of a silver alloy in conjunction with a cladding layer provides good conductivity. The resulting conductivity is sufficient for fabrication of large flat panel displays. In addition, the present invention prevents hillock formation as occurs in prior art processes that use aluminum. Thus, shorts are prevented as compared with prior art processes that use aluminum and planarity of overlying layers is obtained. This results in increased yield as compared with prior art processes that use aluminum. Moreover, the present invention requires a

single patterning step and a single etch step in order to form upper electrode 14. Thus, the present invention does not require two separate patterning steps and two separate etch steps as are required in prior art processes. This results in significant cost savings and increased yield and throughput. Also, the present invention does not use a dry etch process. This results in cost savings and increases in yield and throughput.

10 Referring now to step 109 of Figure 1, a passivation layer is deposited. In one embodiment, the passivation layer is silicon nitride deposited using a plasma enhanced chemical vapor deposition process. Referring now to Figure 10A-10B, the structure of Figure 9A-9B is shown after passivation layer 15 is deposited.

Referring now to step 110 of Figure 1, mask and etch steps are performed. Figures 11A-11B show the structure of Figures 10A-10B after mask and etch steps have formed openings 16-18. It can be seen that passivation layer 15 extends over upper electrode 14 except at openings 17-18.

Gate metal is then deposited as shown by step 111 of Figure 1. In one embodiment, chromium is used as a gate metal. Figures 12A-12B show the structure of Figure 11A-

11B after gate metal layer 20 has been deposited. In an alternate embodiment, gate metal layer 20 is formed by first depositing a tantalum layer and then depositing a chromium layer over the tantalum layer. Passivation layer 5 15 protects upper electrode 14 during the deposition of gate metal layer 20.

Referring now to step 112 of Figure 1, mask and etch steps are performed to form a gate structure. Figure 13A-10 13B show the structure of Figures 11A-11B after mask and etch steps have formed gate structure 21. In the present embodiment, column contact pad 22 allows for contact with upper electrode 14. Passivation layer 15 protects upper electrode 14 during mask and etch steps for forming gate 15 metal structure 21.

Conventional process steps are then used to complete the cathode structure as shown by step 113 of Figure 1. Figure 14A-14B show a completed cathode structure 20 according to one embodiment of the present invention. In one embodiment of the present conventional process steps are used to form cavity 221 and to form exemplary emitter 26 within cavity 221. Mask and etch steps are used to extend opening 16 of Figure 11B so as to expose row 25 contact pad 23. Conventional process steps are also used

to form focusing structure 24 and focus waffle metal 27.
In one embodiment, focus waffle metal 27 is aluminum. In
the present invention, these process steps include ion
bombardment, cavity etch, cone deposition, dielectric
5 deposition, masking and etching of the dielectric layer,
polyimide deposition, etc.

During the process steps for completion of the
cathode, upper electrode 14 is protected by passivation
10 layer 15. This prevents damage to upper electrode 14 as
typically occurs in prior art processes. By preventing
damage to upper electrode 14, upper electrode shorts and
opens are prevented. In addition, because upper electrode
14 is protected, column shorts in the frit seal region are
15 eliminated. Also, because there is less exposed metal as
compared with prior art processes, column to focus waffle
shorts are decreased.

With reference now to Figures 15a-f, a second
20 embodiment of a method for forming an electrode structure
for a display device is shown. As shown by step 101 a
metal alloy layer is deposited. As shown by step 102, a
cladding layer is then deposited. Mask and etch steps are
performed as shown by step 103 to form lower electrodes. A
25 resistor layer is deposited as shown by step 104. A layer

of dielectric is then deposited as shown by step 105. A metal alloy layer is then deposited as shown by step 106. As shown by step 107, a cladding layer is then deposited. Referring to step 108, mask and etch steps are performed
5 for forming upper electrodes. In one embodiment, steps 101-108 are identical to steps 101-108 of Figure 1, producing the structure shown in Figures 9A-9B.

Referring now to step 111 of Figure 15, a gate metal
10 layer is deposited. The gate metal layer is then masked and etched as shown by step 112. Referring now to Figure 16a-b, the structure of Figures 9a-9b is shown after steps 111-112 have been performed so as to form gate structure 1601. In one embodiment, gate structure 1601 is chromium.
15 Alternatively, gate structure 1601 is a layer of chromium deposited over a layer of tantalum.

Continuing with Figure 15, as shown by steps 109-110, a passivation layer is deposited, masked and etched.
20 Figure 16c-16d show the structure of Figure 16a-16b after steps 109-110 have formed passivation layer 1602. In one embodiment, passivation layer 1602 is silicon nitride deposited using a plasma enhanced chemical vapor deposition process. Openings 1620-1621 extend through
25 passivation layer 1602. It can be seen that passivation

layer 1602 extends over gate structure 1601 except at openings 1620-1621.

The cathode structure is then completed as shown by
5 step 113 of Figure 15. Figures 16E-16J illustrate an exemplary method for completing the cathode structure in accordance with one embodiment of the present invention. First an etch step is performed. Figures 16E-16F show the structure of Figures 16C-16D after the etch step has
10 formed cavity 25. A layer of chromium is evaporated over the structure, followed by the deposition of cone material and the deposition of a dielectric layer. In one embodiment, the layer of chromium is thin, having a thickness of approximately 500 Angstroms. The resulting
15 structure is then patterned and etched so as to produce the structure shown in Figures 16G-16H. The structure of Figures 16G-16H shows dielectric material 1654, cone 26, cone material 1653 and chromium 1640. In one embodiment, cone material 1653 is evaporated molybdenum. However, the
20 present invention is well adapted for use of other materials for forming cone 26. Mask and etch steps form opening 1656 that exposes portions of lower electrode 4 so as to form lower contact pad 23. Dielectric removal steps and a halo etch are then performed, followed by formation
25 of polyimide structures and focus waffle metal. Figures

16I-16J show a completed cathode structure that includes polyimide structures 24, focus waffle metal 27 and upper contact pad 22.

5 During the process steps for completion of the cathode, upper electrode 14 is protected by gate metal structure 1601 and by passivation layer 15. This prevents damage to upper electrode 14 as typically occurs in prior art processes. By preventing damage to upper electrode
10 14, upper electrode shorts and opens are prevented. In addition, because upper electrode 14 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, column to focus waffle shorts are
15 decreased.

 With reference now to Figure 17, yet another method for forming an electrode structure for a display device is shown. As shown by step 201, lower electrodes are formed
20 over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203. In one embodiment, steps 201-203 are identical to steps 101-105 of Figure 1.

Continuing with Figure 17, gate metal is deposited as is shown by step 204. In one embodiment, chromium is used as a gate metal.

5 Referring still to Figure 17, upper electrodes are formed as shown by step 205. In the one embodiment, upper electrodes are formed in the same manner as shown in steps 106-108 of Figures 1 and 15. In the present embodiment, upper electrodes are formed by depositing a metal alloy
10 layer that is an aluminum alloy and masking and etching the metal alloy layer. In one specific embodiment, a metal alloy layer is used that a thickness of 500-5000 Angstroms and that includes aluminum (Al) and Neodymium (Nd) with a concentration of from .5 to 6 atomic percent Nd. In
15 another embodiment, an aluminum alloy is used that has a concentration of from .5 to 6 atomic percent Nd and from 0 to 5 atomic percent titanium (Ti).

Figures 18A-18B show substrate 1 after steps 201-205
20 have been performed, forming lower electrodes 4 over substrate 1, resistor layer 5, dielectric layer 6, gate metal layer 1801 and upper electrodes 1810.

Referring back to Figure 17, as shown by step 206,
25 mask and etch steps are then performed so as to

selectively etch gate metal layer 1801 of Figure 18A-18B. More particularly, in the present embodiment, photoresist is deposited over the backplate and is patterned. The backplate is then etched using a wet etch process. Figures 5 18C-18D show the structure of Figures 18A-18B after mask and etch steps have formed gate metal structure 1811.

Referring now to step 207 of Figure 17, a passivation layer is deposited. In one embodiment, the passivation layer is silicon nitride deposited using a plasma enhanced chemical vapor deposition process. 10

Referring now to step 208 of Figure 17, mask and etch steps are performed. Referring now to Figure 18E-18F, the structure of Figure 18C-18D is shown after a passivation layer is deposited, masked and etched to form openings 1820 and 1821 that extend through passivation layer 1830. In one embodiment of the present invention, cavity 1825 is also formed using a HALO etch. It can be seen that 15 passivation layer 1830 extends over upper electrode 1810 except at opening 1820. 20

The cathode structure is then completed as shown by step 209 of Figure 17. Figures 18G-18N illustrate an exemplary method for completing the cathode in accordance 25

with one embodiment of the present invention. Mask and etch steps are performed to form a cavity, shown in Figure 18G as cavity 1825. A layer of chromium is evaporated over the structure, followed by the deposition of cone material and the deposition of a dielectric layer. The resulting structure is then patterned and etched so as to produce the structure shown in Figures 18I-18J. More particularly, cone 1826 and structures 1891 and 1892 are formed. Structures 1891 and 1892 include cone material 1853, chromium material 1840 and dielectric material 1854. Mask and etch steps then form openings that expose portions of lower electrode 4 so as to form lower contact pad 1856 as shown in Figures 18K-18L. Dielectric removal steps and a halo etch are then performed, followed by formation of polyimide structures and focus waffle metal. Figures 18M-18N show a completed cathode structure that includes upper contact pad 1857, focusing structures 1824 and focus waffle metal 1827. In an alternate embodiment of the present invention (not shown) mask and etch steps do not form structure 1892. That is, only structure 1891 is formed.

During the process steps for completion of the cathode, upper electrode 1810 is protected by passivation layer 1830. This prevents damage to upper electrode 1810

as typically occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region
5 are eliminated. Also, because there is less exposed metal as compared with prior art processes, column to focus waffle shorts are decreased.

With reference now to Figure 19, yet another method
10 for forming an electrode structure for a display device is shown. As shown by step 201 lower electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203.

15

Continuing with Figure 19, gate metal is deposited as is shown by step 204. In one embodiment, chromium is used as a gate metal.

20 Referring still to Figure 19, a tantalum layer is deposited as shown by step 250. Upper electrodes are then formed as shown by step 205. In the present embodiment, upper electrodes are formed using an aluminum alloy. In one embodiment, the metal alloy has a thickness of 500-
25 5000 Angstroms. In one specific embodiment, an aluminum

alloy is used that includes aluminum (Al) and Neodymium (Nd). In the present embodiment, the aluminum alloy has an concentration of from .5 to 6 atomic percent Nd. In another embodiment, an aluminum alloy is used that has a
5 concentration of from .5 to 6 atomic percent Nd and from 0 to 5 atomic percent titanium (Ti).

Figures 18a-18b show substrate 1 after steps 201-205 and 250 have been performed, forming a gate metal layer
10 1801, a tantalum layer 1802, and upper electrodes 1810. In one embodiment, lower electrode 4 is a row electrode and upper electrode 1810 is a column electrode. However, alternatively, the present invention is well adapted to use of lower electrode 4 as a column electrode and upper
15 electrode 1810 as a row electrode.

Referring back to Figure 19, as shown by step 252, mask and etch steps are then performed so as to selectively etch tantalum layer 1802 and gate metal layer
20 1801 of Figure 20A-20B. More particularly, in the present embodiment, photoresist is deposited over the backplate and is patterned. The backplate is then etched using a wet etch process. Figures 20C-20D show the structure of Figures 20A-20B after mask and etch steps have formed gate
25 metal structure 1811 and tantalum structure 1812.

Referring now to step 207 of Figure 19, a passivation layer is deposited. In one embodiment, the passivation layer is silicon nitride deposited using a plasma enhanced
5 chemical vapor deposition process.

Referring now to step 208 of Figure 19, mask and etch steps are performed. Referring now to Figure 20E-20F, the structure of Figure 20C-20D is shown after a passivation
10 layer is deposited, masked and etched to form opening 1820 that extends through passivation layer 1830 and tantalum structure 1812. In one embodiment of the present invention, a halo etch is also performed, forming cavity 1825. It can be seen that passivation layer 1830 extends
15 over upper electrode 1810 except at opening 1820. Passivation layer 1830 protects upper electrode 1810 during subsequent process steps.

The cathode structure is then completed as shown by
20 step 209 of Figure 19. Figures 20G-20L illustrate an exemplary method for completing the cathode structure in accordance with one embodiment of the present invention. A layer of chromium is evaporated over the structure, followed by the deposition of cone material and the
25 deposition of a dielectric layer. The resulting structure

is then patterned and etched so as to produce the structure shown in Figures 20G-20H. The structure of Figures 20G-20H includes dielectric material 1854, cone 1826, cone material 1853 and chromium segment 1840. In one embodiment, cone material 1853 is evaporated molybdenum. However, the present invention is well adapted for use of other materials for forming cone 1826. Mask and etch steps then form openings 1856-1857 that expose portions of lower electrode 4 and upper electrode 1810 so as to form lower contact pad 1823 and upper contact pad 1822 as shown in Figures 20I-20J. Dielectric removal steps and a halo etch are then performed, followed by formation of polyimide structures and focus waffle metal. Figures 20K-20L show a completed cathode structure that includes polyimide structures 1824 and focus waffle metal 1827.

During the process steps for completion of the cathode, upper electrode 1810 is protected by passivation layer 1830. This prevents damage to upper electrode 1810 as typically occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal

as compared with prior art processes, column to focus
wafile shorts are decreased.

With reference now to Figure 21, yet another method
5 for forming an electrode structure for a display device is
shown. As shown by steps 201, lower electrodes are formed
over a substrate. A resistor layer and a dielectric layer
are then deposited over the lower electrodes as shown by
steps 202-203.

10

Continuing with Figure 21, gate metal is deposited as
is shown by step 204. In one embodiment, chromium is used
as a gate metal. Upper electrodes are then formed as
shown by step 205. In the present embodiment, upper
15 electrodes are formed of an aluminum alloy. In one
embodiment, steps 201-205 are identical to steps 201-205
of Figure 17.

Referring now to Figures 22A-22B, a substrate 1 is
20 shown after steps 201-205 have formed a gate metal layer
1801 and upper electrodes 1810 that overlie dielectric
layer 6, resistor layer 5 and lower electrode 4.

Referring now to step 207 of Figure 21, a passivation
25 layer is deposited. In one embodiment, the passivation

layer is silicon nitride deposited using a plasma enhanced chemical vapor deposition process. Alternatively, a tantalum layer can be used.

5 Referring back to Figure 21, as shown by step 260, mask and etch steps are then performed. In one embodiment, a two step etch process is used whereby the passivation layer is etched using a first etch step and the gate metal layer is etched in a second etch step. The
10 first mask and etch step etches through the passivation layer and etches through the gate metal layer. Figures 22C-22D show the structure of Figures 22A-22B after mask and etch steps have formed gate metal structure 1811 and passivation layer 1830.

15

The cathode structure is then completed as shown by step 209 of Figure 21. Figures 22E-22N illustrate an exemplary method for completing the cathode in accordance with one embodiment of the present invention. A
20 dielectric layer is deposited over the structure of Figures 22C-22D. The dielectric layer 2250 is then patterned and etched to form the structure shown in Figures 22E-22F. During the etch process, passivation layer 1830 acts as an etch stop. A cavity etch is then

performed. Figures 22G-22H show the structure of Figures 22E-22F after the cavity etch has formed cavity 1825.

A layer of Molybdenum is then deposited, using a
5 sputter deposition process. A layer of cone material is then deposited over the layer of Molybdenum. In one embodiment, a cone material that is evaporated molybdenum is used. However, the present invention is well adapted for use of other materials for forming a cone. A layer of
10 dielectric is then deposited. The resulting structure is then patterned and etched so as to produce the structure shown in Figures 22I-22J. The structure of Figures 22I-22J includes Molybdenum structure 2252, cone 2226, cone material 2253 and dielectric layer 2254. Mask and etch
15 steps then form openings 2256-2257 shown in Figures 22K-22L. Referring now to Figures 22M-22N, dielectric removal steps and a halo etch are then performed, producing contact pads 2222 and 2223, followed by formation of polyimide focusing structures 2224 and focus waffle metal
20 2227.

During the process steps for completion of the cathode, upper electrode 1810 is protected by passivation layer 1830. This prevents damage to upper electrode 1810
25 as typically occurs in prior art processes. By preventing

damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal
5 as compared with prior art processes, upper electrode to focus waffle shorts are decreased.

With reference now to Figures 23-24, yet another method for forming an electrode structure for a display
10 device is shown. As shown by step 201 of Figure 23, lower electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203. A gate metal layer is deposited as shown by step 204, followed by the
15 formation of upper electrodes as shown by step 205. An etch step is then performed to form a gate structure as shown by step 206 followed by etch step 2301 to form a cavity.

20 In the present embodiment, upper electrodes are formed by the deposition and etch of a metal alloy layer. In one embodiment, the metal alloy is an aluminum alloy that has a thickness of 500-5000 Angstroms. In one specific embodiment, an aluminum alloy is used that
25 includes aluminum (Al) and Neodymium (Nd). In the present

embodiment, the aluminum alloy has an concentration of
from .5 to 6 atomic percent Nd. In another embodiment, an
aluminum alloy is used that has a concentration of from .5
to 6 atomic percent Nd and from 0 to 5 atomic percent
5 titanium (Ti).

Referring to Figure 24A-24B, a substrate 1 is shown
after steps 201-206 have formed lower electrodes 4,
resistor layer 5, dielectric layer 6, gate metal structure
10 1811 and upper electrodes 1810. Etch step 2301 forms
cavity 2425.

Continuing with Figure 23, a layer of sputtered
molybdenum is then deposited as shown by step 2302. A
15 layer of evaporated molybdenum is then deposited as shown
by step 2303, followed by the deposition of a layer of
sputtered molybdenum as shown by step 2304. Referring now
to Figure 24C-24D, the structure of Figures 24A-24B is
shown after steps 2302-2304 form sputtered molybdenum
20 layer 2401, evaporated molybdenum layer 2402, sputtered
molybdenum layer 2403 and cone 2426.

Referring back to Figure 23, as shown by step 2305,
mask and etch steps are then performed. Figures 24E-24F
25 show the structure of Figures 24C-24D after mask and etch

steps have formed molybdenum structures 2430-2431 and an opening 2422 that extends to the top of lower electrode 4. In one embodiment, mask and etch step 2305 includes two separate mask and etch steps, a first mask and etch step
5 that etches sputtered molybdenum layer 2403, evaporated molybdenum 2402 and molybdenum layer 2401, and a second mask and etch step that etches through dielectric layer 6 and resistor layer 5 to form opening 2422.

10 Referring to step 2306 of Figure 23, a dielectric layer is deposited. In one embodiment, the dielectric layer is silicon dioxide.

Referring now to step 2307 of Figure 23, a
15 passivation layer is deposited. In one embodiment, the passivation layer is silicon nitride deposited using a plasma enhanced chemical vapor deposition process. Figures 24G-24H show the structure of Figures 24E-24F after the deposition of dielectric layer 2440 and passivation layer
20 2441.

Referring now to step 2308, mask and etch steps are then performed. Referring now to Figures 24I-24J step 2308 forms openings 2450-2452 that extend through passivation
25 layer 2441.

As shown in step 2309, Focusing structures are formed. A dry etch process is then performed as shown by step 2310. Referring now to Figures 24K-24L, steps 2309-
5 2310 form polyimide focusing structures 2424 and openings 2461-2463 that extend through dielectric layer 2440. Opening 2462 extends to the top surface of lower contact pad 4, forming lower contact pad 2423. Referring now to Figure 24M, in the present embodiment, focus waffle metal
10 2427 is formed over focusing structures 2424.

Another etch is performed as shown by step 2311 to complete the structure. Referring now to Figures 24M-24N, etch step 2311 is shown to extend opening 2461 and opening
15 2463 of Figures 24K-24L through sputtered molybdenum layer 2403 and evaporated molybdenum layer 2402, forming contact pad 2422 and removing that portion of sputtered molybdenum layer 2403 and evaporated molybdenum layer 2402 that overlie cone 2426.

20

In the process shown in Figures 23-24, dielectric layer 2440 and passivation layer 2441 protect upper electrodes 1810, preventing damage to upper electrode 1810 as typically occurs in prior art processes. By preventing
25 damage to upper electrode 1810, upper electrode shorts and

opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, upper electrode to
5 focus waffle shorts are decreased.

With reference now to Figures 25-26, yet another method for forming an electrode structure for a display device is shown. As shown by step 201 of Figure 25, lower
10 electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower electrodes as shown by steps 202-203. A gate metal layer is deposited as shown by step 204, followed by the formation of upper electrodes as shown by step 205. Mask
15 and etch step 206 forms a gate structure. A cavity is then etched as shown by step 2301.

A layer of sputtered molybdenum, a layer of evaporated molybdenum, and a second layer of sputtered
20 molybdenum are then deposited as shown by steps 2302-2304. In one embodiment, steps 201-206 and 2301-2304 are identical to steps 201-206 and 2301-2304 of Figure 23.

Referring now to step 2501 of Figure 25, a mask and
25 etch step is performed that selectively etches both

sputtered molybdenum layers and the evaporated molybdenum layer. In the present embodiment, mask and etch step 2501 removes all of that portion of the sputtered molybdenum layers and the evaporated molybdenum layers that overlie the region where the upper electrode contact pad is to be formed. That is, in the present embodiment, structure 2431 shown in figure 24F is also removed during etch step 2501.

10 Referring to step 2502 of Figure 25, a dielectric layer is deposited. In one embodiment, the dielectric layer is silicon dioxide.

Referring now to Figures 26A-26B, a substrate 1 is shown after steps 201-206, 2301-2304, and 2501-2502 of Figure 25 have formed dielectric layer 2600, molybdenum layer 2401, evaporated molybdenum layer 2402, and sputtered molybdenum layer 2403 such that cone 2426 is formed. Also shown are gate metal layer 1811 and upper electrodes 1810 that overlie dielectric layer 6, resistor layer 5 and lower electrode 4.

Referring now to step 2503 of Figure 25, mask and etch steps are performed. In one embodiment, mask and etch step 2503 includes three mask and etch steps, a first

mask and etch step that produces the structure shown in
Figures 26C-26D, a second mask and etch step that produces
the structure shown in Figures 26E-26F and a third mask
and etch step that produces the structure shown in Figures
5 26G-26H. Referring now to Figures 26G-26H, the third mask
and etch step forms an opening that extends to lower
electrode 4, forming contact pad 2643. In the present
embodiment, first and second etches are dry etches and the
third etch is a wet etch. However, the present invention
10 is well adapted to the use of different mask and etch
processes for producing the structure shown in Figures
26G-26H.

As shown in step 2504, Focusing structures are
15 formed. Referring to Figure 26I, in the present
embodiment, focus waffle metal 2627 is formed over
focusing structures 2624. As shown by step 2505 of Figure
25, an etch step is performed so as to further etch the
remaining dielectric layer. In one embodiment, etch step
20 2504 uses a dry etch process. Referring now to Figures
26I-26J, step 2504 forms polyimide structures 2624 while
step 2505 forms contact pad 2642.

Another etch is then performed as shown by step 2506
25 to complete the structure. In the present embodiment, as

shown in Figures 26K-26L, etch step 2506 removes evaporated molybdenum layer 2553 and sputtered molybdenum layers 2552 and 2554.

5 Upper electrode 1810 is protected by dielectric layer 2600, preventing damage to upper electrode 1810 as typically occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode
10 1810 is protected, column shorts in the frit seal region are eliminated. Also, because there is less exposed metal as compared with prior art processes, upper electrode to focus waffle shorts are decreased.

15 With reference now to Figures 27-28, yet another method for forming an electrode structure for a display device is shown. As shown by step 201 of Figure 27, lower electrodes are formed over a substrate. A resistor layer and a dielectric layer are then deposited over the lower
20 electrodes as shown by steps 202-203. A gate metal layer is deposited as shown by step 204. Upper electrodes are then formed as shown by step 205. As shown by step 206, mask and etch steps are then performed to form a gate structure. Mask and etch steps are then performed as
25 shown by step 2301 to form a cavity. In one embodiment,

steps 201-206 and 2301 are identical to steps 201-206 and 2301 of Figure 23.

Continuing with Figure 27, a layer of evaporated
5 chromium is then deposited as shown by step 2701, followed
by the deposition of a layer of evaporated molybdenum as
shown by step 2702. A dielectric layer is then deposited
as shown by step 2703.

10 Referring to Figure 28A-28B, a substrate 1 is shown
after steps 201-206 have formed lower electrodes 4,
resistor layer 5, dielectric layer 6, gate metal structure
1811 and upper electrodes 1810. Etch step 2301 forms
cavity 2425. Steps 2701-2703 result in the formation of
15 evaporated chromium layer 2830, evaporated molybdenum
layer 2831, and dielectric layer 2832.

Referring back to Figure 27, as shown by step 2704,
mask and etch steps are then performed. Referring now to
20 Figures 28C-28D, step 2704 etches through dielectric layer
2832, molybdenum layer 2831, evaporated chromium layer
2830 and partially etches upper electrodes 1810.

Continuing with Figure 27, as shown by step 2705,
25 another etch step is performed that etches dielectric

layer 6 and resistor layer 5, forming the structure shown in Figures 28E-28F. Step 2706 exposes a portion of lower electrode 4 so as to form contact pad 2823.

5 Continuing with Figure 27, as shown by step 2706, the focusing structure is formed. Referring now to Figures 28G-H, focusing structure 2824 is shown to be formed. Referring now to Figure 28G, in the present embodiment, focus waffle metal 2827 is formed over focusing structures
10 2824.

Continuing with Figure 27, as shown by step 2707, an etch step is performed. Referring now to Figures 28I-28J, step 2707 is shown to remove dielectric layer 2832 and to
15 partially remove a portion of dielectric layer 6.

Another etch is then performed as shown by step 2708 to complete the structure. Figures 28K-28L show the structure of Figure 28I-28J after step 2708 has been
20 performed. In the present embodiment, etch step 2708 removes evaporated molybdenum layer 2831.

During process steps 2704-2708, upper electrode 1810 is protected by evaporated chromium layer 2830. This
25 prevents damage to upper electrode 1810 as typically

occurs in prior art processes. By preventing damage to upper electrode 1810, upper electrode shorts and opens are prevented. In addition, because upper electrode 1810 is protected, column shorts in the frit seal region are
5 eliminated. Also, because there is less exposed metal as compared with prior art processes, column to focus waffle shorts are decreased.

The foregoing descriptions of specific embodiments of
10 the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The
15 embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications are suited to the particular use
20 contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

CLAIMS:

1. An electrode structure for a display device comprising:

5 a plurality of first electrodes disposed over a backplate, said plurality of first electrodes further comprising a metal alloy;

a dielectric layer disposed over said plurality of first electrodes; and

10 a plurality of second electrodes, said plurality of second electrodes disposed over said dielectric layer, said plurality of second electrodes further comprising said metal alloy.

15 2. An electrode structure for a display as recited in Claim 1 wherein said plurality of first electrodes are row electrodes and said plurality of second electrodes are column electrodes.

20 3. An electrode structure for a display as recited in Claim 1 wherein said plurality of first electrodes are column electrodes and said plurality of second electrodes are row electrodes.

4. An electrode structure for a display as recited in Claim 1 wherein said metal alloy comprises an aluminum alloy.

5 5. An electrode structure for a display as recited in Claim 4 wherein said aluminum alloy comprises aluminum and neodymium.

10 6. An electrode structure for a display as recited in Claim 5 wherein said aluminum alloy comprises from approximately .5 atomic percent neodymium to approximately 6 atomic percent neodymium.

15 7. An electrode structure for a display as recited in Claim 5 wherein said aluminum alloy further comprises titanium.

20 8. An electrode structure for a display as recited in Claim 7 wherein said aluminum alloy comprises up to approximately 5 atomic percent titanium.

9. An electrode structure for a display as recited in Claim 1 wherein said plurality of first electrodes further comprise:
25 a cladding layer disposed over said metal alloy.

10. An electrode structure for a display as recited in Claim 9 wherein said cladding layer comprises molybdenum and tungsten.

5

11. An electrode structure for a display as recited in Claim 1 wherein said metal alloy comprises a silver alloy.

10

12. An electrode structure for a display as recited in Claim 11 wherein said silver alloy comprises silver and palladium.

15

13. An electrode structure for a display as recited in Claim 12 wherein said silver alloy comprises from approximately .5 atomic percent palladium to approximately 2 atomic percent palladium.

20

14. An electrode structure for a display as recited in Claim 12 wherein said silver alloy further comprises copper.

15. An electrode structure for a display as recited in Claim 14 wherein said silver alloy comprises from

approximately .5 atomic percent copper to approximately 2
atomic percent copper.

16. An electrode structure for a display as recited
5 in Claim 12 wherein said silver alloy further comprises
titanium.

17. An electrode structure for a display as recited
in Claim 16 wherein said silver alloy comprises up to
10 approximately 2 atomic percent titanium.

18. An electrode structure for a display as recited
in Claim 1 further comprising:

a passivation layer disposed over said plurality of
15 second electrodes.

19. An electrode structure for a display as recited
in Claim 18 wherein said passivation layer comprises
silicon nitride.

20

20. An electrode structure for a display as recited
in Claim 1 further comprising a resistor layer overlying
said plurality of first electrodes, said dielectric layer
overlying said resistor layer.

21. A method for forming an electrode structure of a display comprising:

a) depositing a layer of metal alloy over a backplate;

5 b) depositing a cladding layer over said layer of metal alloy such that said layer of cladding overlies said layer of metal alloy; and

c) etching said layer of metal alloy and said cladding layer using a wet etch process so as to form a
10 plurality of electrodes.

22. A method for forming an electrode structure of a display as recited in Claim 20 wherein step a) and step b) are performed sequentially in a single sputtering tool.

15

23. A method for forming an electrode structure of a display as recited in Claim 21 wherein said metal alloy comprises an aluminum alloy.

20

24. A method for forming an electrode structure of a display as recited in Claim 23 wherein said aluminum alloy further comprises aluminum and neodymium.

25. A method for forming an electrode structure of a
25 display as recited in Claim 24 wherein said aluminum alloy

comprises from approximately .5 atomic percent neodymium to approximately 6 atomic percent neodymium.

26. A method for forming an electrode structure of a
5 display as recited in Claim 24 wherein said metal alloy further comprises titanium.

27. A method for forming an electrode structure of a
display as recited in Claim 26 wherein said aluminum alloy
10 comprises up to approximately 5 atomic percent titanium.

28. A method for forming an electrode structure of a
display as recited in Claim 21 wherein said cladding layer
comprises molybdenum and tungsten.

15

29. A method for forming an electrode structure of a
display as recited in Claim 21 wherein said metal alloy
comprises a silver alloy.

20 30. A method for forming an electrode structure of a display as recited in Claim 29 wherein said silver alloy comprises silver and palladium.

31. A method for forming an electrode structure of a
25 display as recited in Claim 30 wherein said silver alloy

comprises from approximately .5 atomic percent palladium to approximately 2 atomic percent palladium.

32. A method for forming an electrode structure of a display as recited in Claim 30 wherein said silver alloy further comprises titanium.

33. A method for forming an electrode structure of a display as recited in Claim 32 wherein said silver alloy comprises up to approximately 2 atomic percent titanium.

34. A method for forming an electrode structure of a display as recited in Claim 29 wherein said silver alloy further comprises from approximately .5 atomic percent copper to approximately 2 atomic percent copper.

35. A method for forming an electrode structure of a display as recited in Claim 34 wherein said silver alloy comprises up to approximately 2 atomic percent titanium.

36. A method for forming an electrode structure of a display comprising:

a) depositing a first metal alloy layer over a backplate;

b) masking and etching said first metal alloy layer so as to form a plurality of first electrodes;

c) depositing a resistor layer over said plurality of first electrodes;

5 d) depositing a dielectric layer over said resistor layer;

e) depositing a second metal alloy layer over said dielectric layer;

10 f) masking and etching said second metal alloy layer so as to form a plurality of second electrodes;

g) depositing a layer of silicon nitride over said plurality of second electrodes, said layer of silicon nitride adapted to protect said plurality of second electrodes during subsequent process steps.

15

37. A method for forming an electrode structure of a display as recited in Claim 36 further comprising:

a1) disposing a cladding layer over said first metal alloy layer such that said layer of cladding overlies said
20 first metal alloy layer.

38. A method for forming an electrode structure of a display as recited in Claim 36 wherein step b) further comprises:

b1) etching said first metal alloy layer and said layer of cladding sequentially in a single sputtering tool.

5 39. A method for forming an electrode structure of a display as recited in Claim 36 further comprising:

a1) disposing a cladding layer over said second metal alloy layer such that said layer of cladding overlies said second metal alloy layer.

10

40. A method for forming an electrode structure of a display as recited in Claim 36 wherein step f) further comprises:

15 f1) etching said second metal alloy layer and said layer of cladding sequentially in a single sputtering tool.

20 41. A method for forming an electrode structure of a flat panel display as recited in Claim 36 wherein steps b) and f) are performed using an etchant that includes nitric acid and phosphoric acid and acetic acid and water so as to form angled edges on each of said plurality of electrodes.

25

42. A method for forming an electrode structure of a flat panel display as recited in Claim 36 wherein said first metal alloy layer and said second metal alloy layer comprise an aluminum alloy.

5

43. A method for forming an electrode structure of a flat panel display as recited in Claim 36 wherein said first metal alloy layer and said second metal alloy layer comprise a silver alloy.

10

44. The electrode structure of Claim 37 wherein said cladding layer further comprises molybdenum and tungsten.

45. A method for forming an electrode structure of a display comprising:

15

a) forming a plurality of first electrodes;

b) depositing a resistor layer over said plurality of first electrodes;

c) depositing a dielectric layer over said resistor layer;

20

d) forming a plurality of second electrodes; and

e) depositing a passivation layer over said plurality of second electrodes, said passivation layer adapted to protect said plurality of second electrodes during

25 subsequent process steps.

46. A method for forming an electrode structure as recited in claim 45 wherein said passivation layer further comprises a layer of silicon nitride.

5 47. A method for forming an electrode structure as recited in claim 46 further comprising the step of forming a gate structure, said gate structure disposed over said layer of silicon nitride.

10 48. A method for forming an electrode structure as recited in claim 46 further comprising the step of forming a gate structure, said gate structure disposed between said plurality of second electrodes and said layer of silicon nitride.

15 49. A method for forming an electrode structure as recited in claim 46 further comprising the step of forming a gate structure, said gate structure disposed between said dielectric layer and said plurality of second
20 electrodes.

50. A method for forming an electrode structure as recited in claim 49 wherein said step of forming a gate structure further comprises the step of depositing a layer

of gate metal, said layer of gate metal masked and etched prior to the deposition of said layer of silicon nitride.

51. A method for forming an electrode structure as
5 recited in claim 49 wherein said step of forming a gate structure further comprises the step of depositing a layer of gate metal, said layer of gate metal masked and etched after the deposition of said layer of silicon nitride.

10 52. A method for forming an electrode structure as recited in claim 49 further comprising the step of forming a tantalum structure, said tantalum structure disposed between said gate structure and said plurality of second electrodes.

15 53. A method for forming an electrode structure as recited in claim 46 further comprising the step of depositing a dielectric layer prior to the step of depositing said layer of silicon nitride.

20 54. An electrode structure for a display device comprising:

- a) a plurality of first electrodes;
- b) a resistor layer disposed over said plurality of
25 first electrodes;

c) a dielectric layer disposed over said resistor layer;

d) a plurality of second electrodes disposed over said dielectric layer; and

5 e) a passivation layer disposed over said plurality of second electrodes.

55. An electrode structure for a display as recited in claim 54 wherein said passivation layer comprises a
10 layer of silicon nitride.

56. An electrode structure for a display as recited in claim 55 further comprising:

f) a gate structure, said gate structure disposed
15 over said layer of silicon nitride.

57. An electrode structure for a display as recited in claim 55 further comprising:

f) a gate structure, said gate structure disposed
20 between said plurality of second electrodes and said layer of silicon nitride.

58. An electrode structure for a display as recited in claim 55 further comprising:

f), a gate structure, said gate structure disposed between said dielectric layer and said plurality of second electrodes.

5 59. An electrode structure for a display as recited in claim 58 further comprising:

g) a tantalum structure, said tantalum structure disposed between said gate structure and said plurality of second electrodes.

10

60. An electrode structure for a display as recited in claim 55 further comprising:

g) a dielectric layer disposed between said plurality of second electrodes and said layer of silicon nitride.

15

61. A method for forming an electrode structure of a display comprising:

a) forming a plurality of first electrodes;

b) depositing a resistor layer over said plurality of

20 first electrodes;

c) depositing a first dielectric layer over said resistor layer;

d) forming a plurality of second electrodes; and

e) depositing a second dielectric layer over said
25 plurality of second electrodes, said second dielectric

layer adapted to protect said plurality of second electrodes during subsequent process steps.

62. A method for forming an electrode structure as
5 recited in claim 61 further comprising the step of depositing a first sputtered molybdenum layer over said plurality of second electrodes.

63. A method for forming an electrode structure as
10 recited in claim 62 further comprising the step of depositing an evaporated molybdenum layer over said first sputtered molybdenum layer and depositing a second sputtered molybdenum layer over said evaporated molybdenum layer, said second dielectric layer disposed over said
15 second layer of evaporated molybdenum.

64. A method for forming an electrode structure of a display comprising:

- a) forming a plurality of first electrodes;
- 20 b) depositing a resistor layer over said plurality of first electrodes;
- c) depositing a first dielectric layer over said resistor layer;
- d) forming a plurality of second electrodes; and

e) depositing a layer of evaporated chromium over said plurality of second electrodes, said layer of evaporated chromium adapted to protect said plurality of second electrodes during subsequent process steps.

5

65. A method for forming an electrode structure as recited in claim 64 further comprising the step of depositing an a second dielectric layer, said second dielectric layer disposed over said layer of evaporated chromium.

10

66. A method for forming an electrode structure as recited in claim 65 further comprising the step of depositing an evaporated molybdenum layer over said layer of evaporated chromium, said second dielectric layer disposed over said layer of evaporated molybdenum.

15

67. An electrode structure for a display device comprising:

20

- a) a plurality of first electrodes;
- b) a resistor layer disposed over said plurality of first electrodes;
- c) a first dielectric layer disposed over said resistor layer;

d) a plurality of second electrodes disposed over said dielectric layer; and

e) a second dielectric layer disposed over said plurality of second electrodes.

5

68. An electrode structure for a display as recited in claim 67 wherein said dielectric layer comprises a layer of silicon dioxide.

10

69. An electrode structure for a display as recited in claim 68 further comprising:

f) an evaporated molybdenum layer disposed between said sputtered molybdenum layer and said second dielectric layer.

15

ELECTRODE STRUCTURE AND METHOD FOR FORMING ELECTRODE
STRUCTURE FOR A FLAT PANEL DISPLAY

5

ABSTRACT OF THE DISCLOSURE

An electrode structure for a display that includes lower electrodes and upper electrodes. In one embodiment, lower and upper electrodes are formed of either an aluminum alloy or a silver alloy. In another embodiment, upper and lower electrodes are formed using a metal alloy layer over which a cladding layer is deposited. A silicon nitride passivation layer is used to protect the upper electrodes from damage in subsequent process steps. Various other materials and structures are also disclosed that protect the upper electrodes from damage in subsequent process steps.

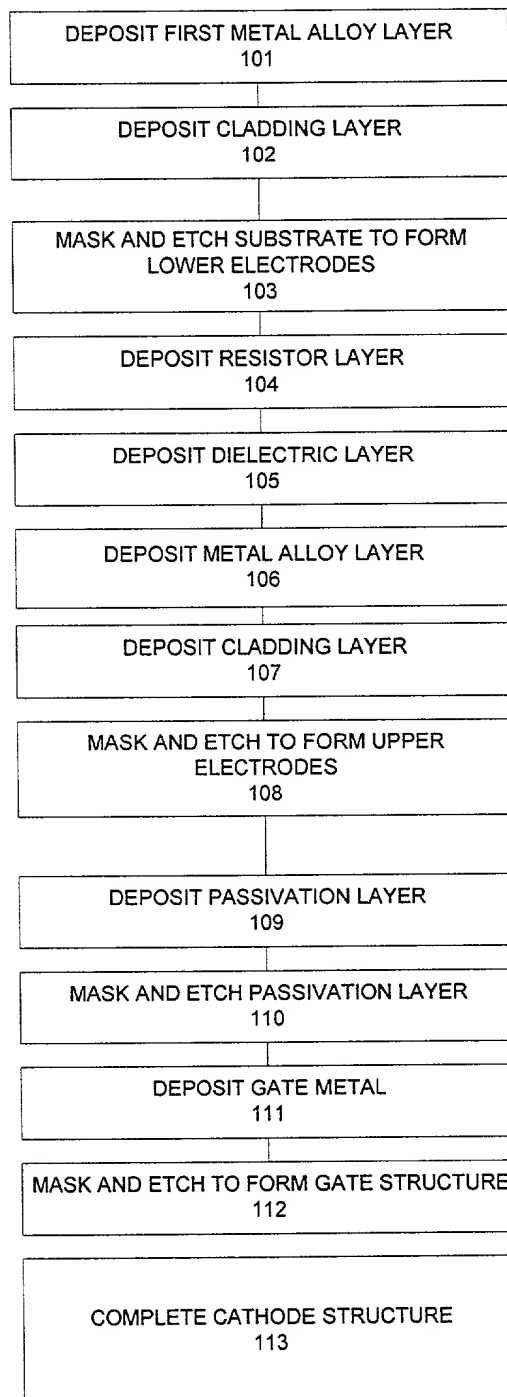


FIG. 1

[illegible]

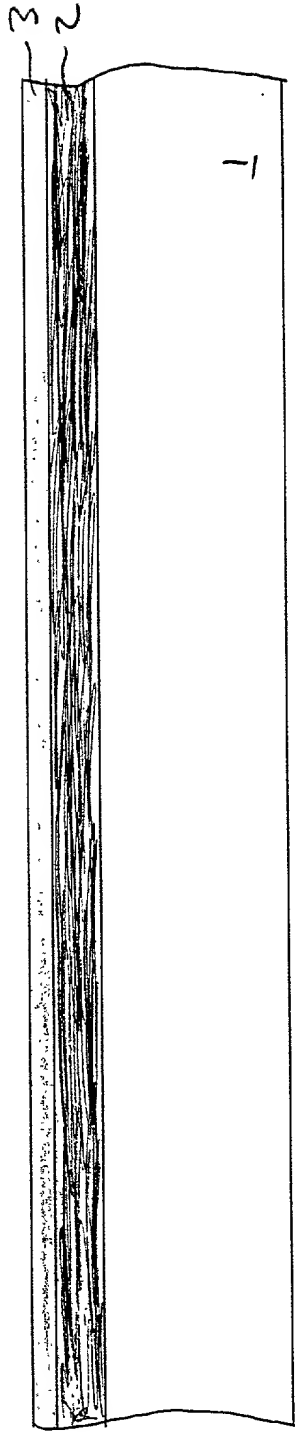


FIG. 3

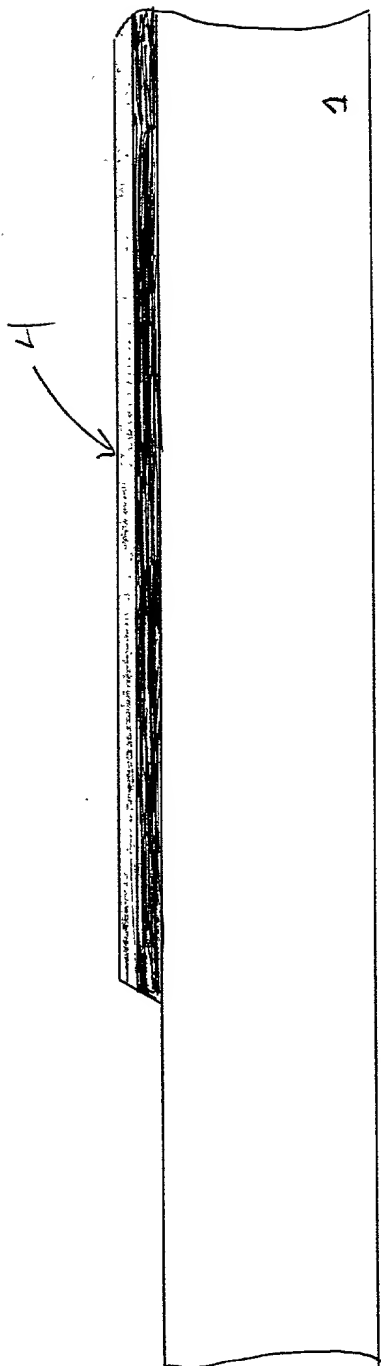


Fig. 4A

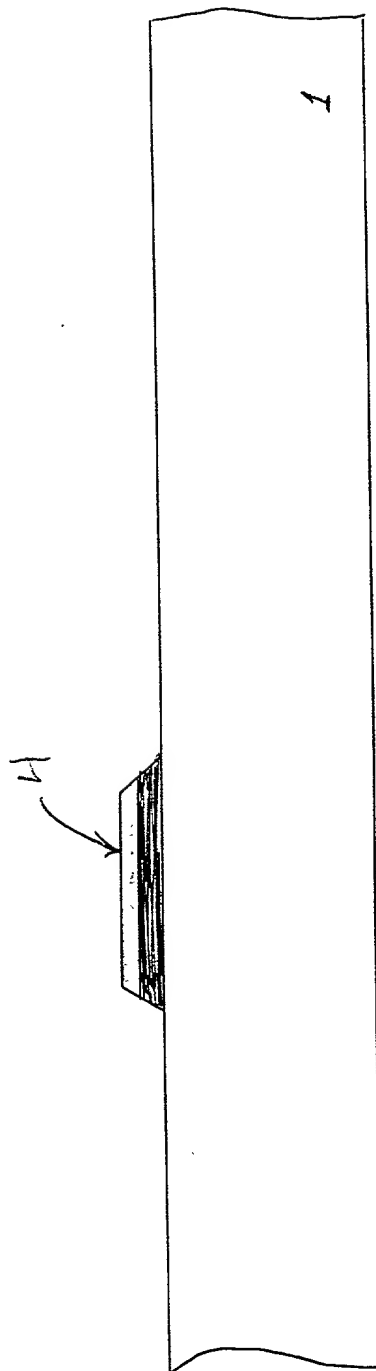


FIG. 4B

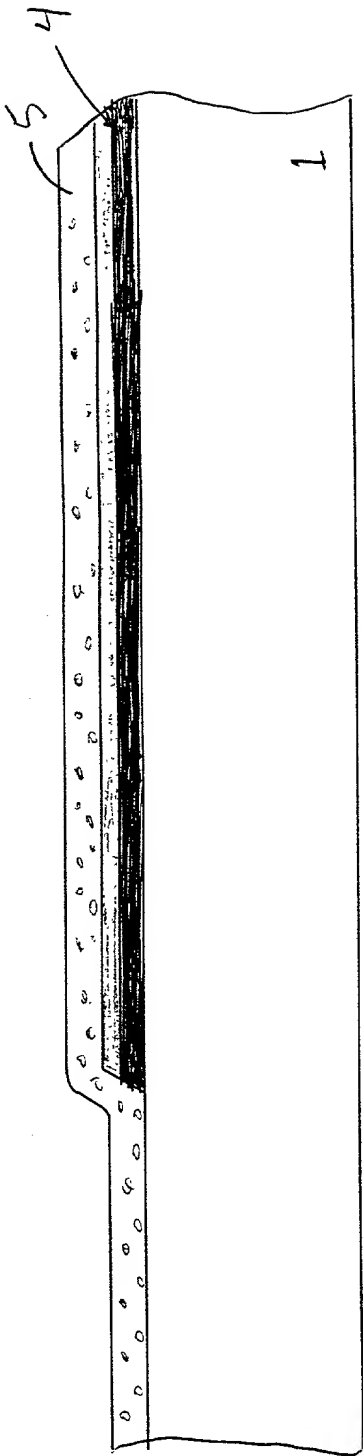


FIG. 5A

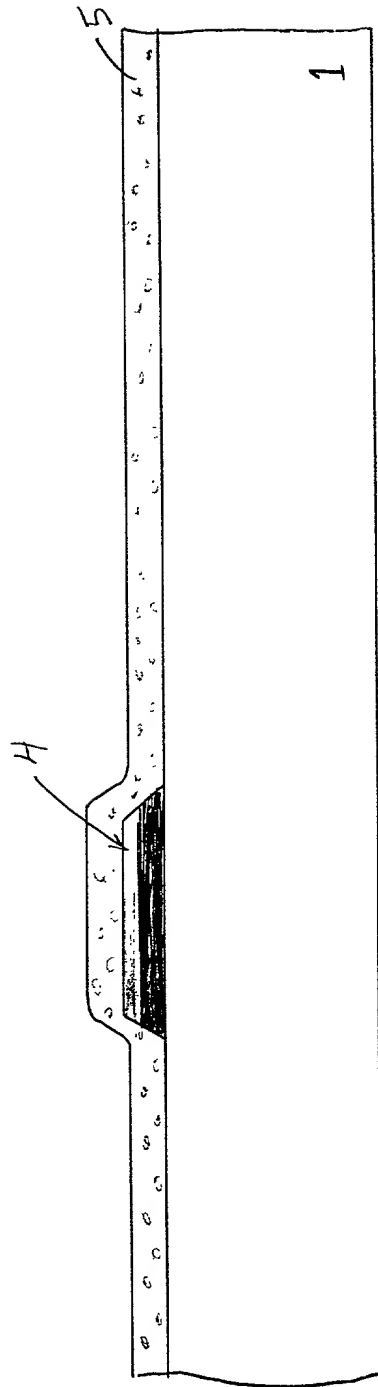


FIG. 5B

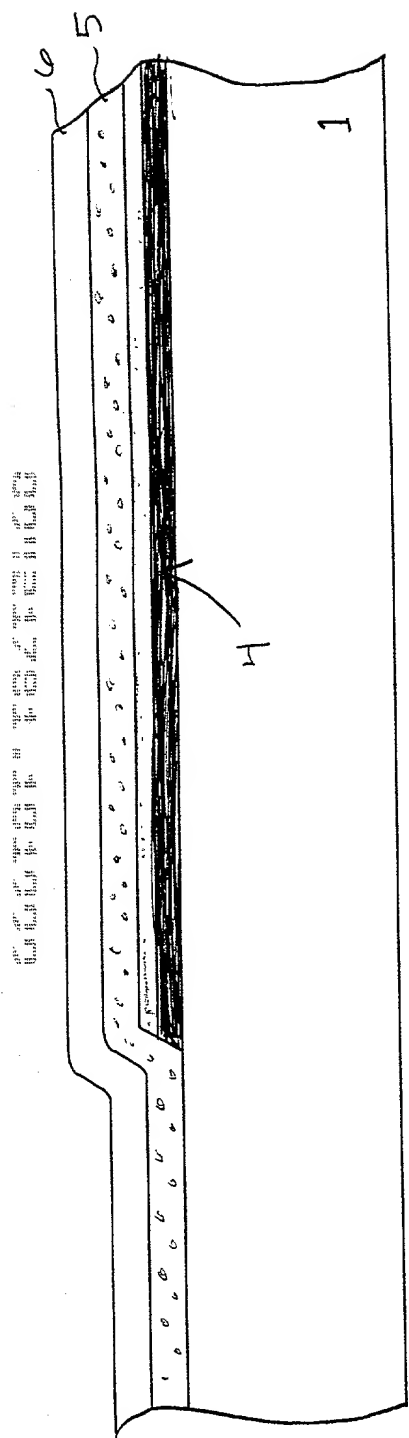


FIG. 6A

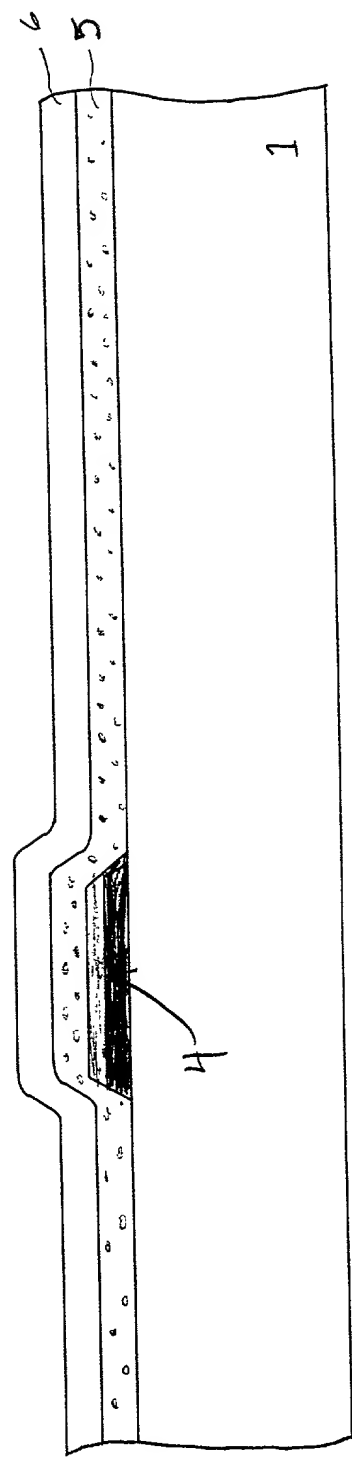


FIG. 6B

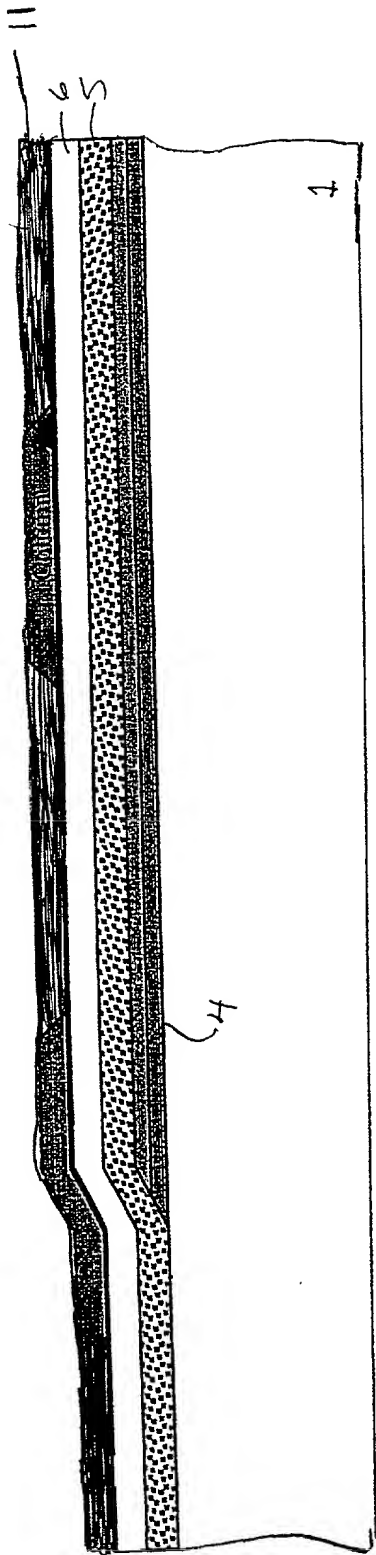


FIG. 7A

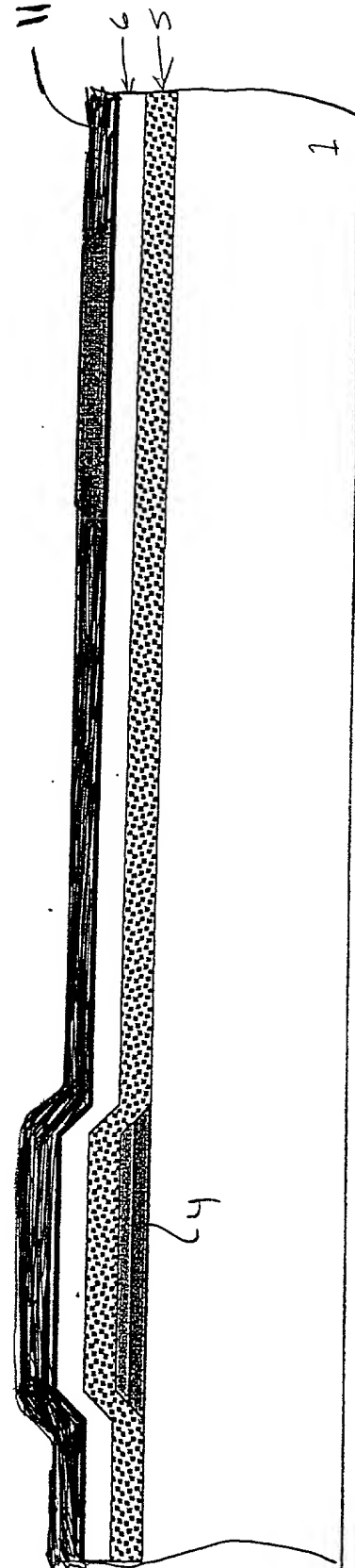


FIG. 7B

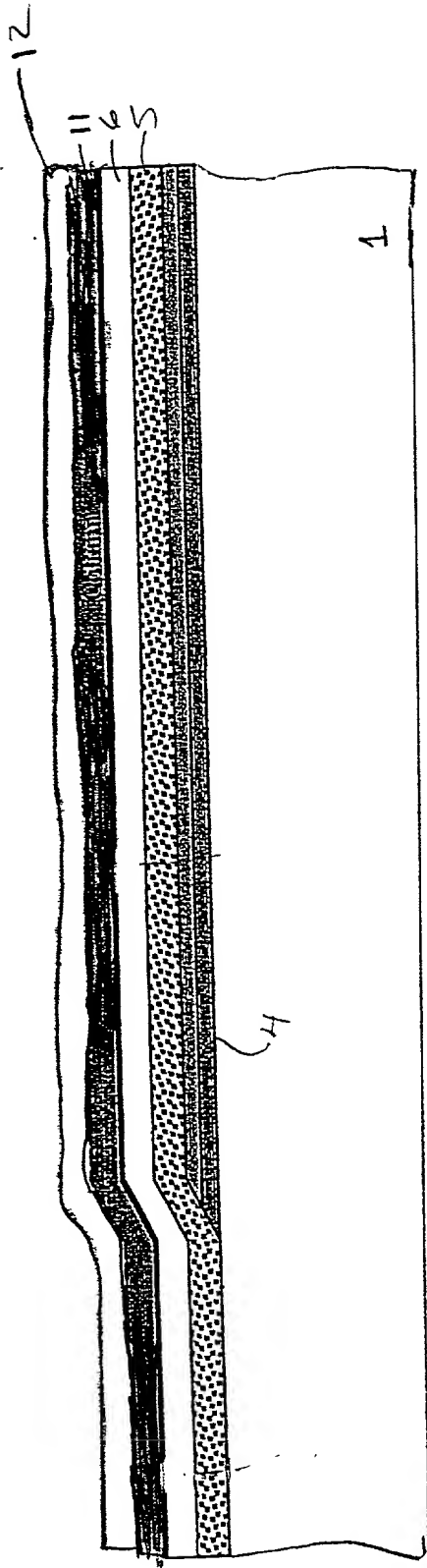


FIG. 8A

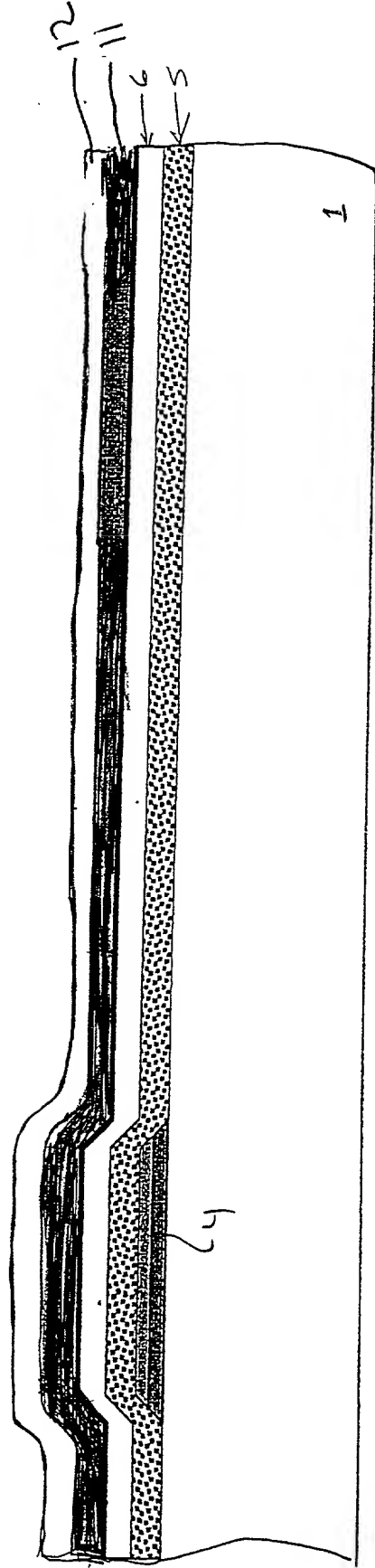


FIG. 8B

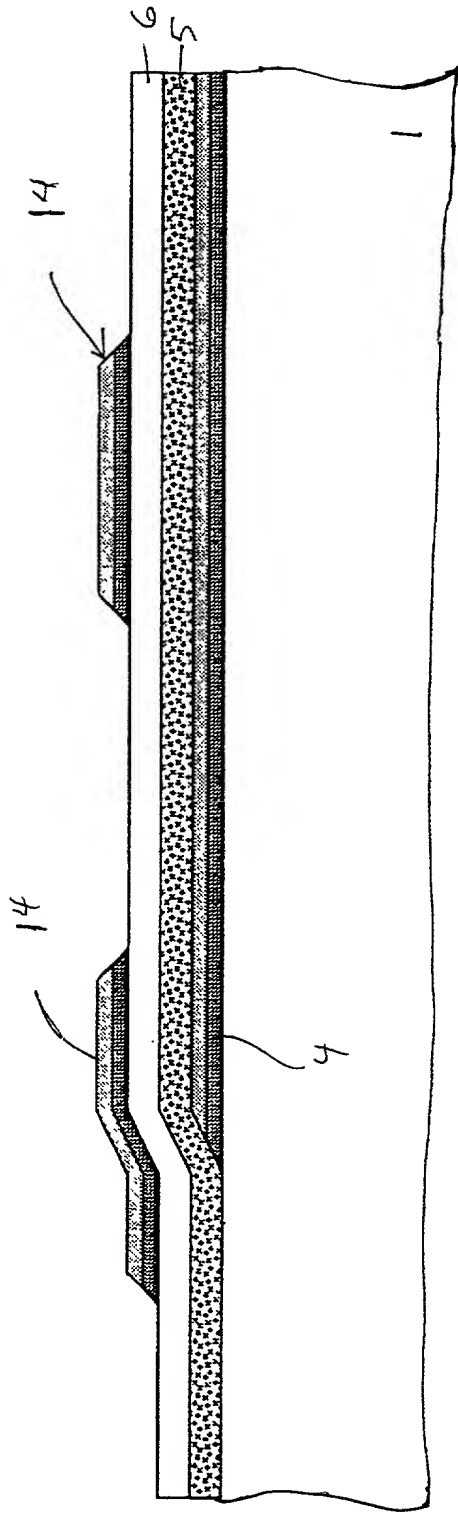


FIG. 9A

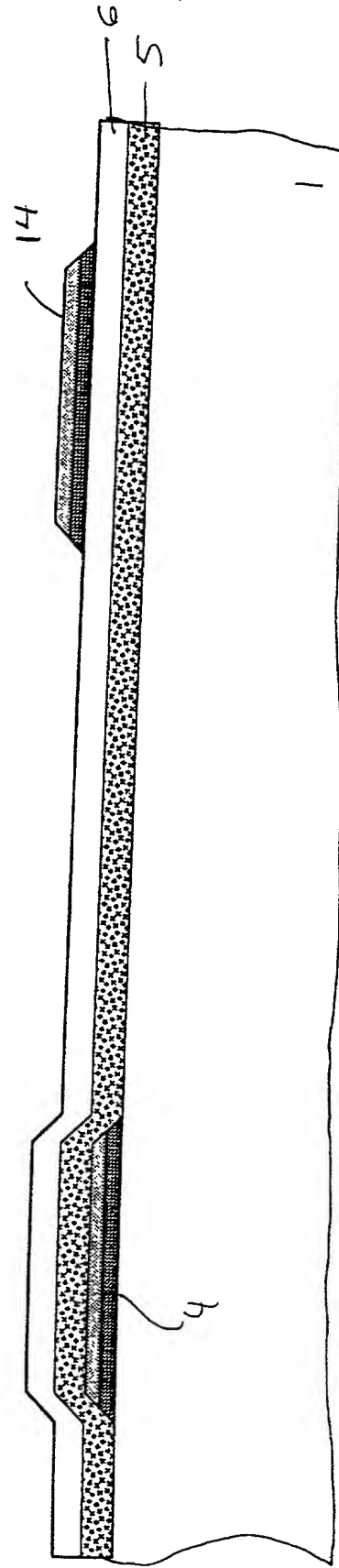


FIG. 9B

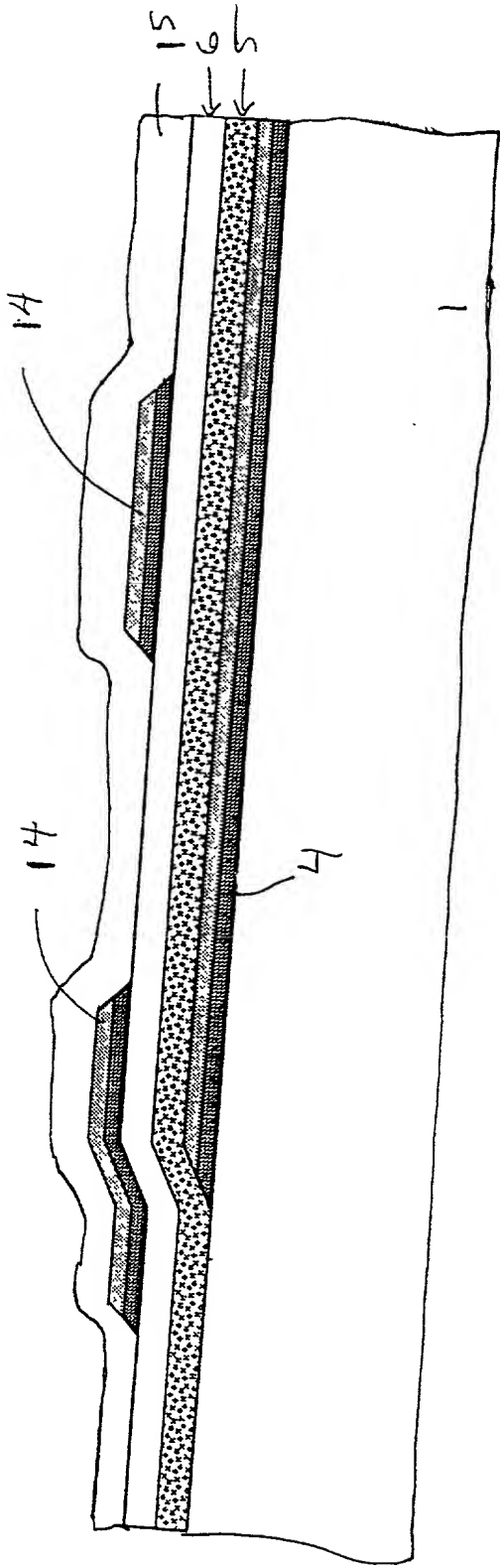


FIG. 10A

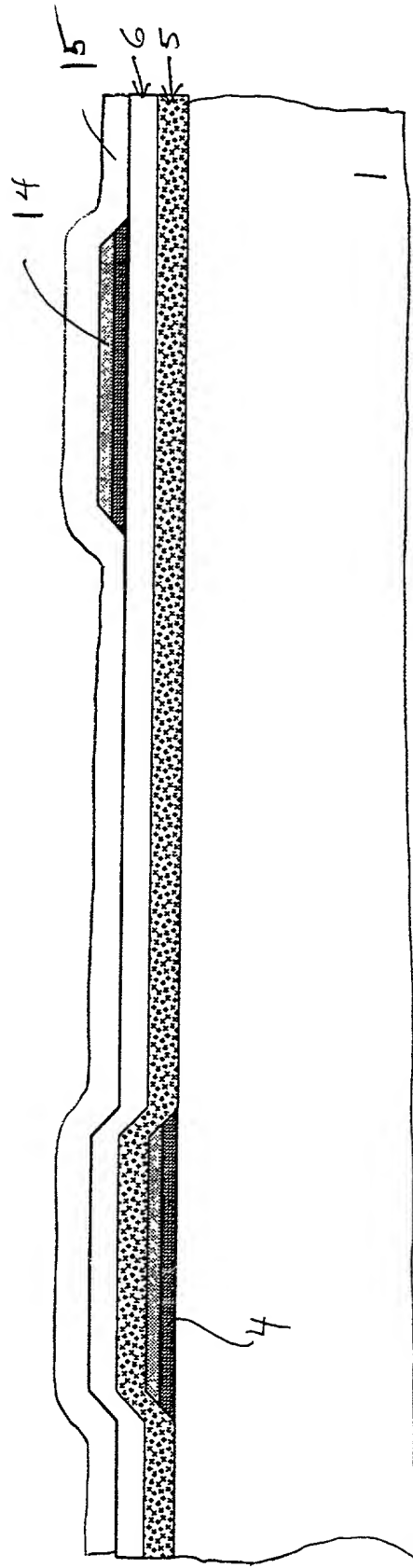


FIG. 10B

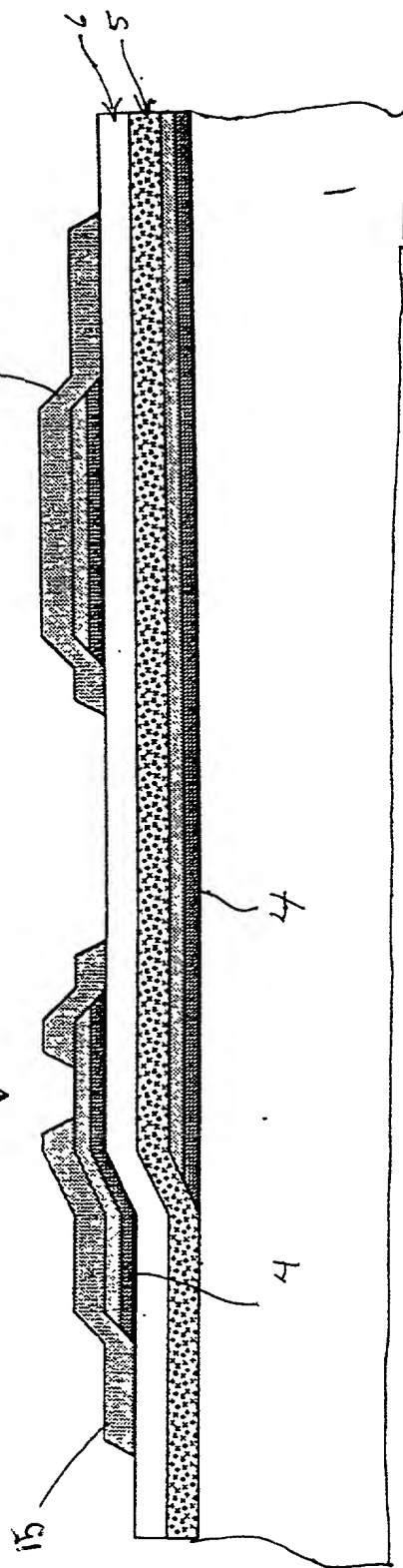
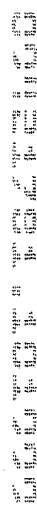


Fig. 11A

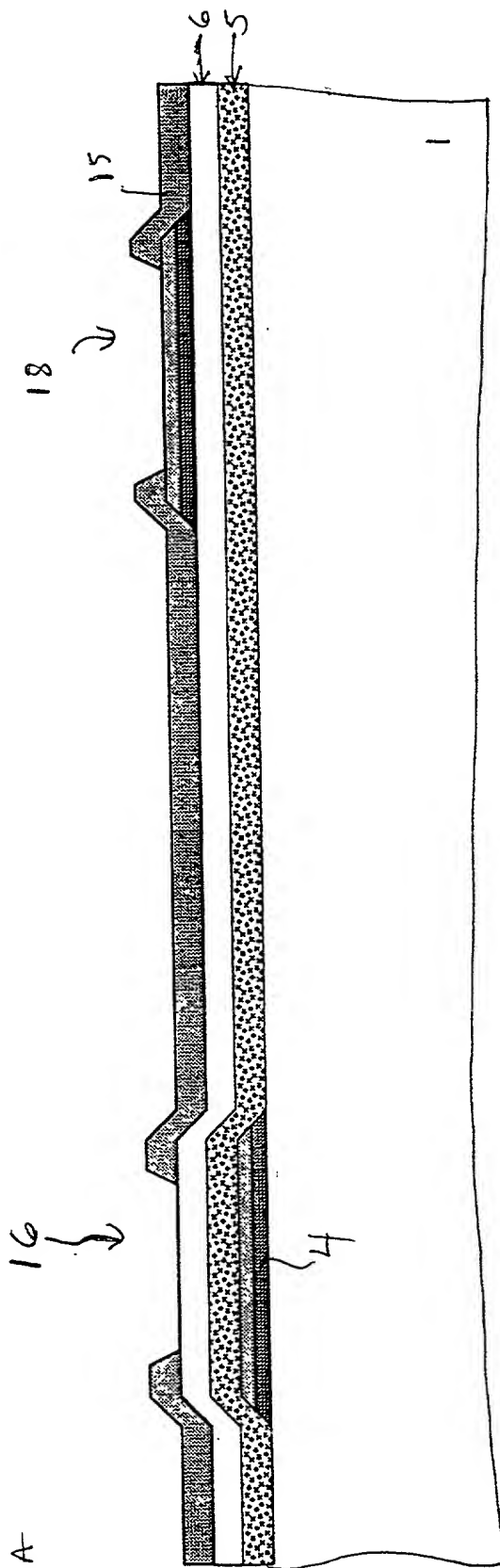


FIG. 11B

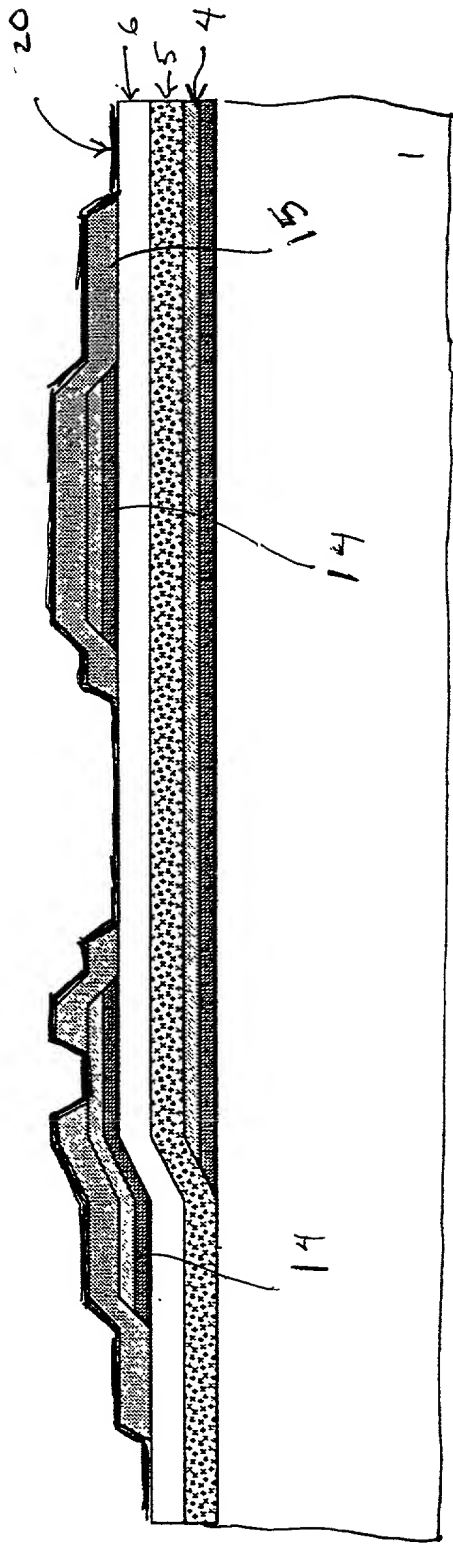


FIG. 12A

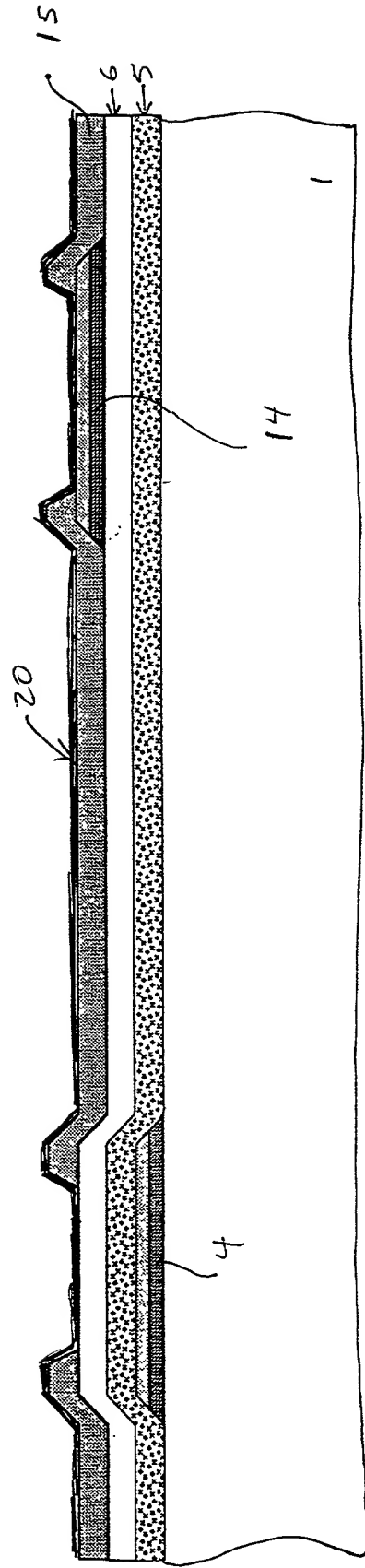


FIG. 12B

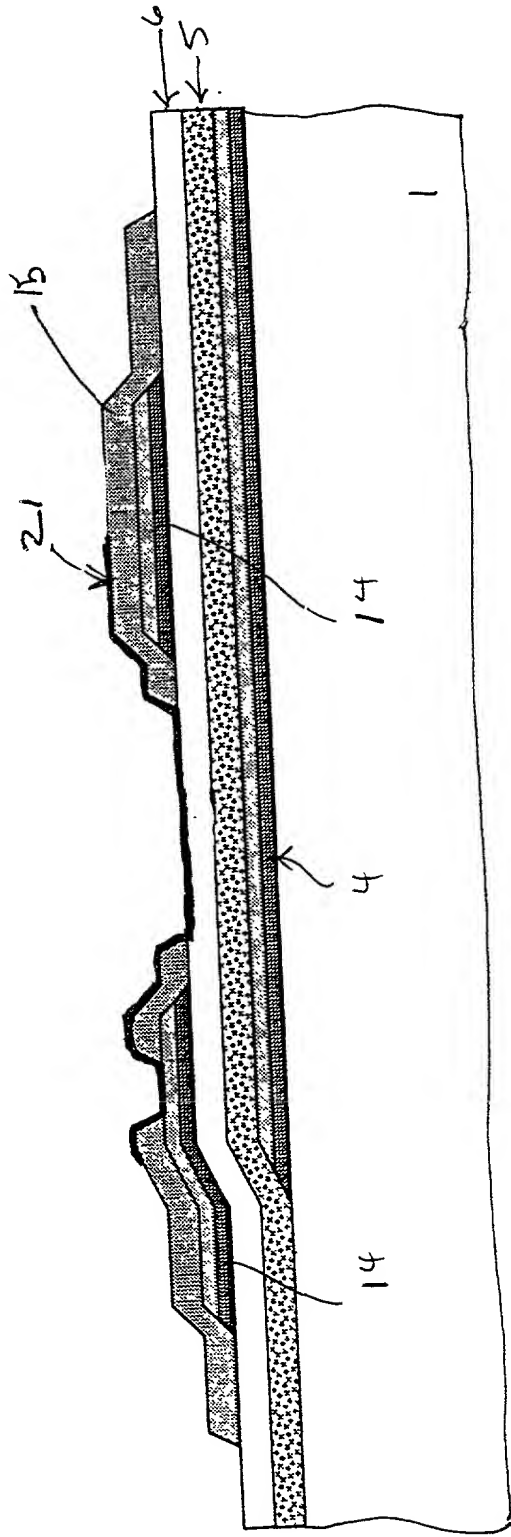


FIG. 13A

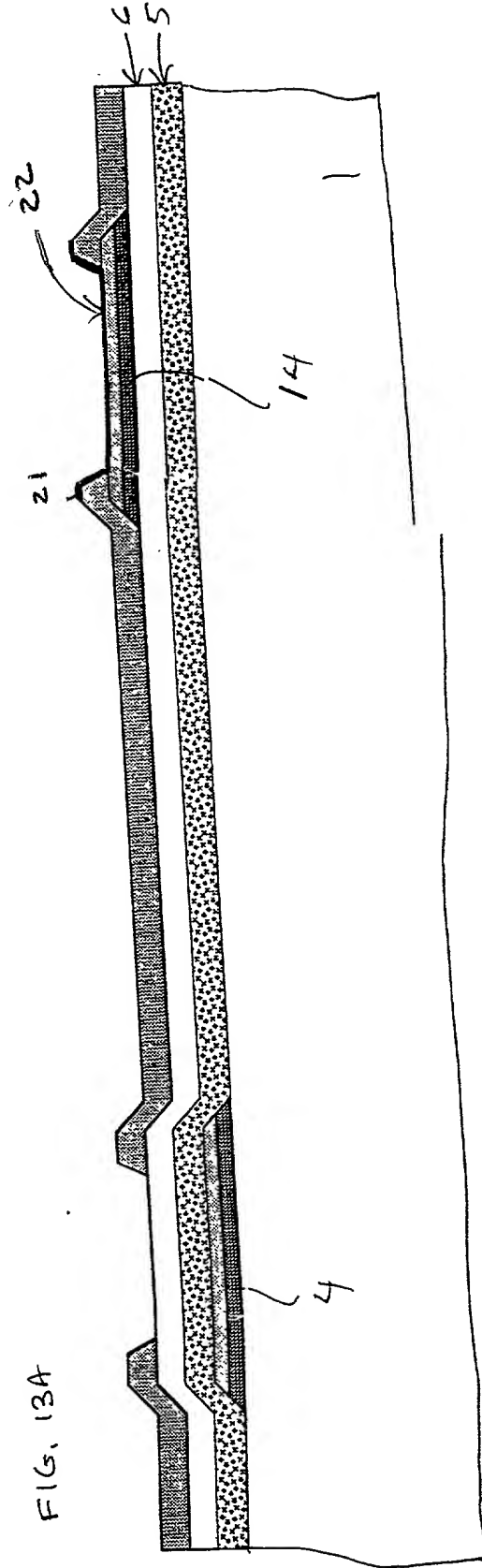
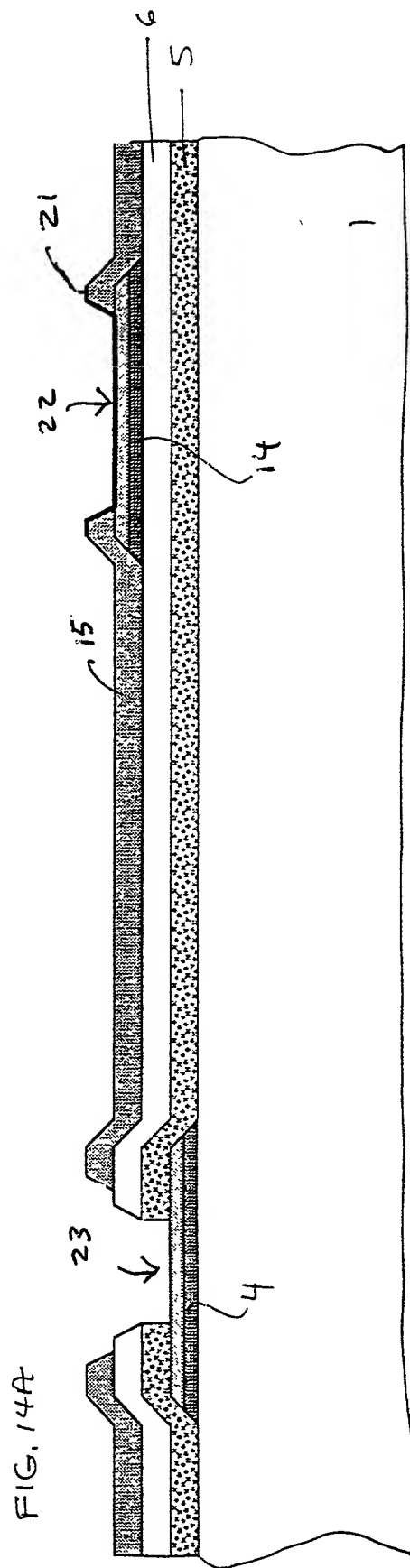
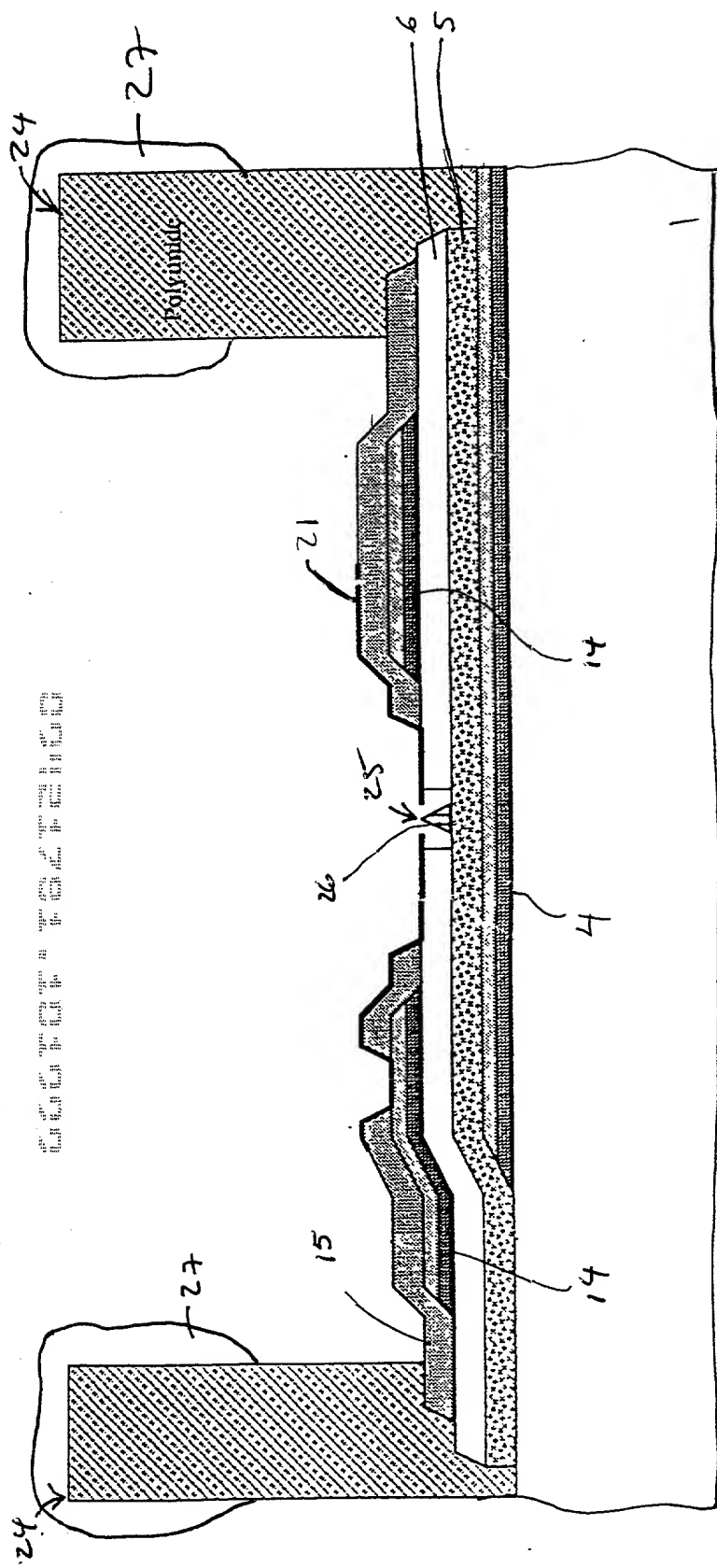


FIG. 13B



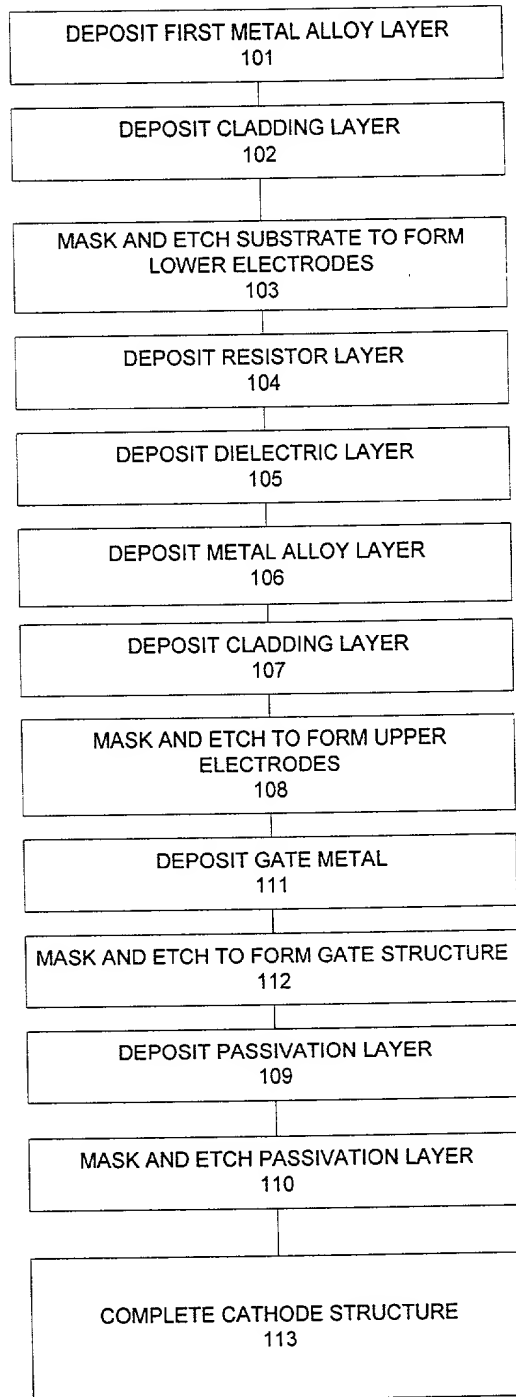


FIG. 15

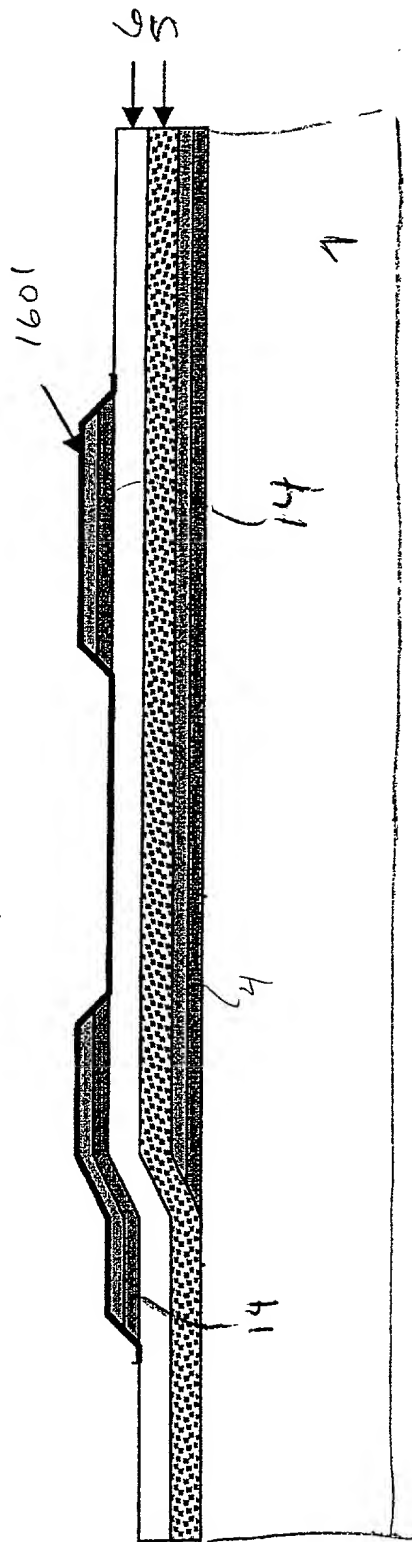


FIG. 16A

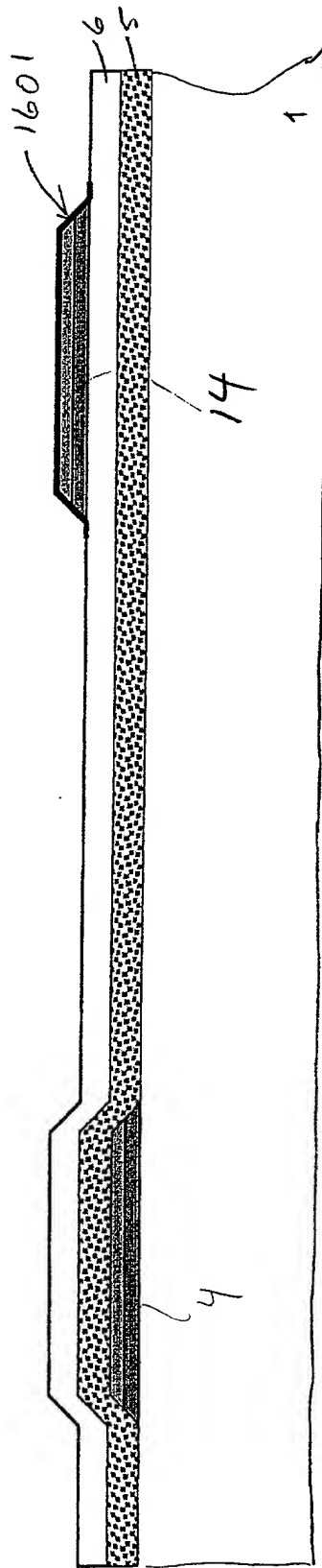


FIG. 16B

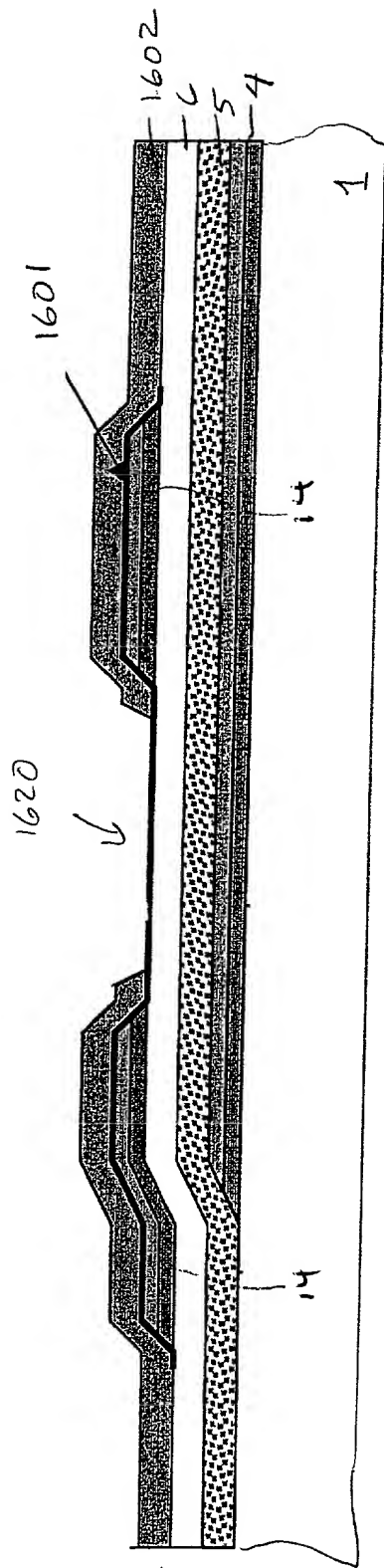


FIG. 16C

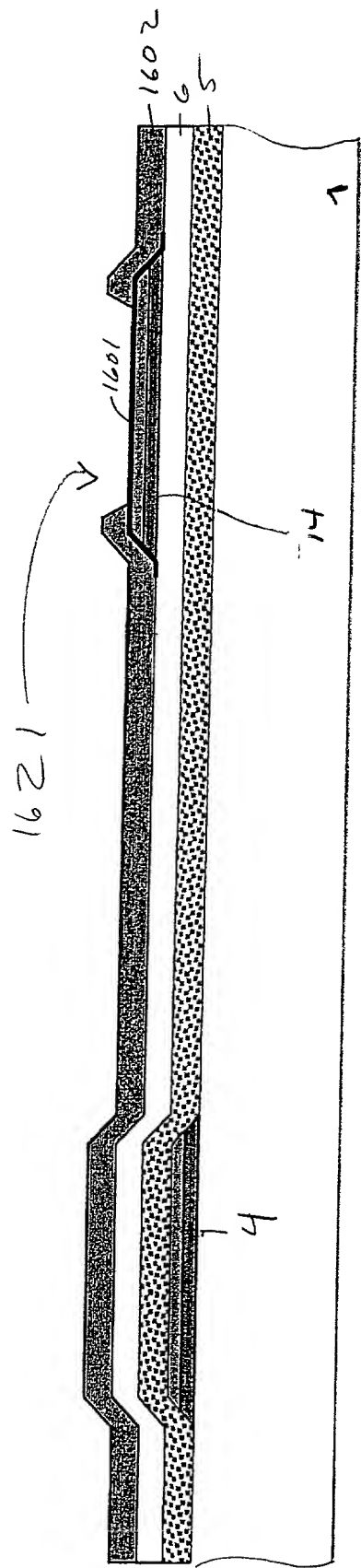


FIG. 16D

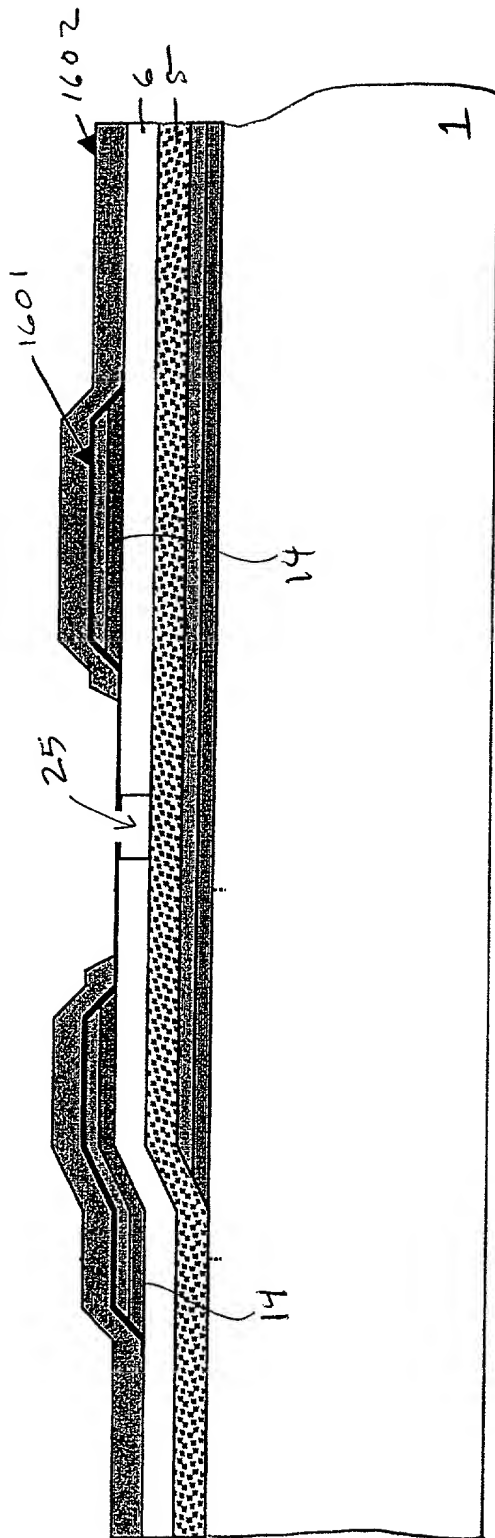


FIG. 16E

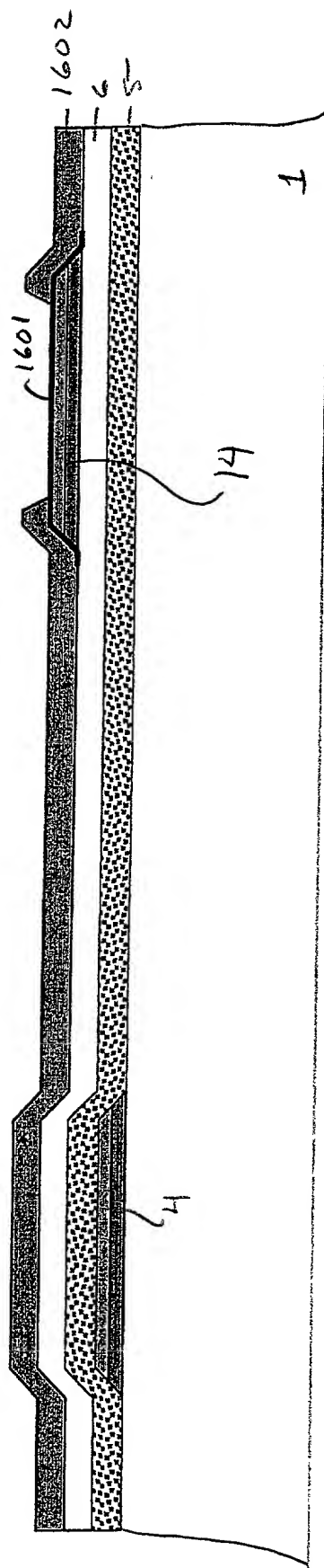


FIG. 16F

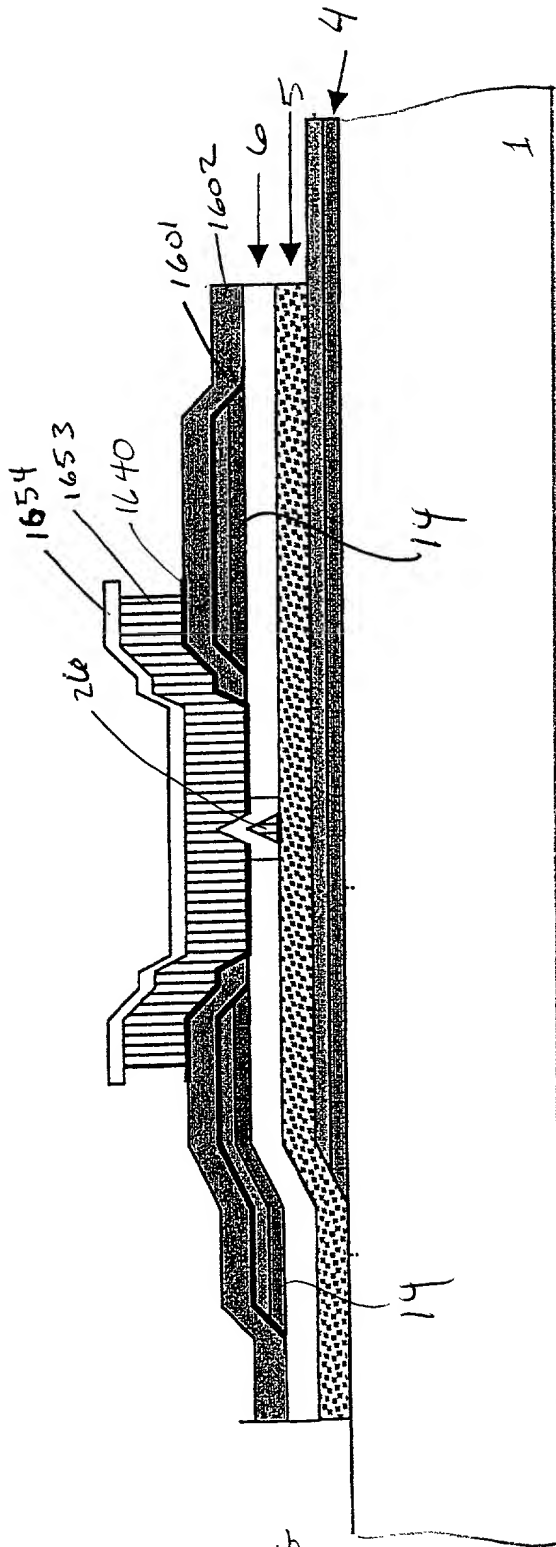


FIG 16G

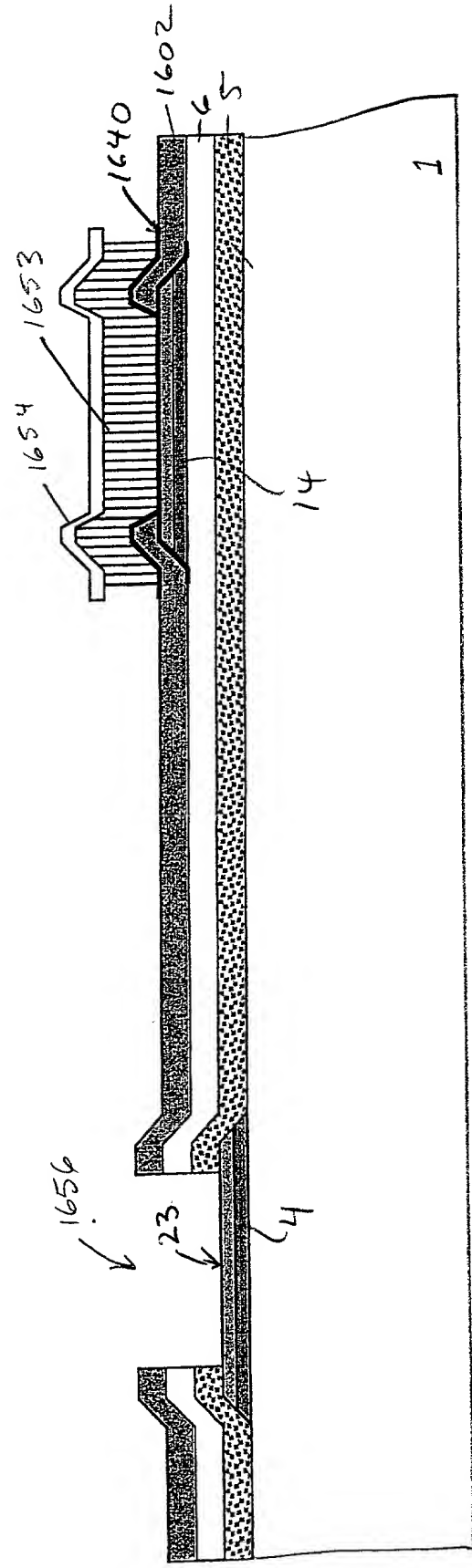


FIG 16H

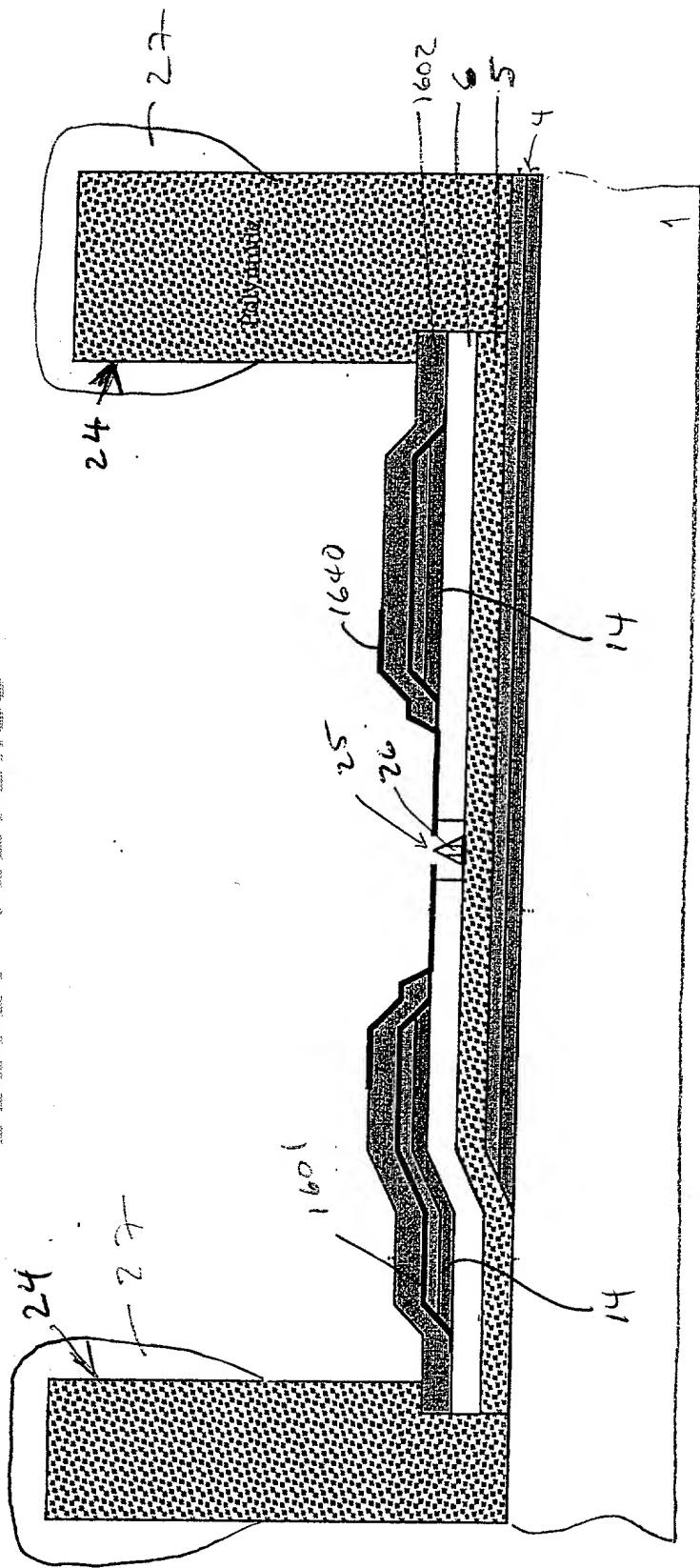


FIG 16 I

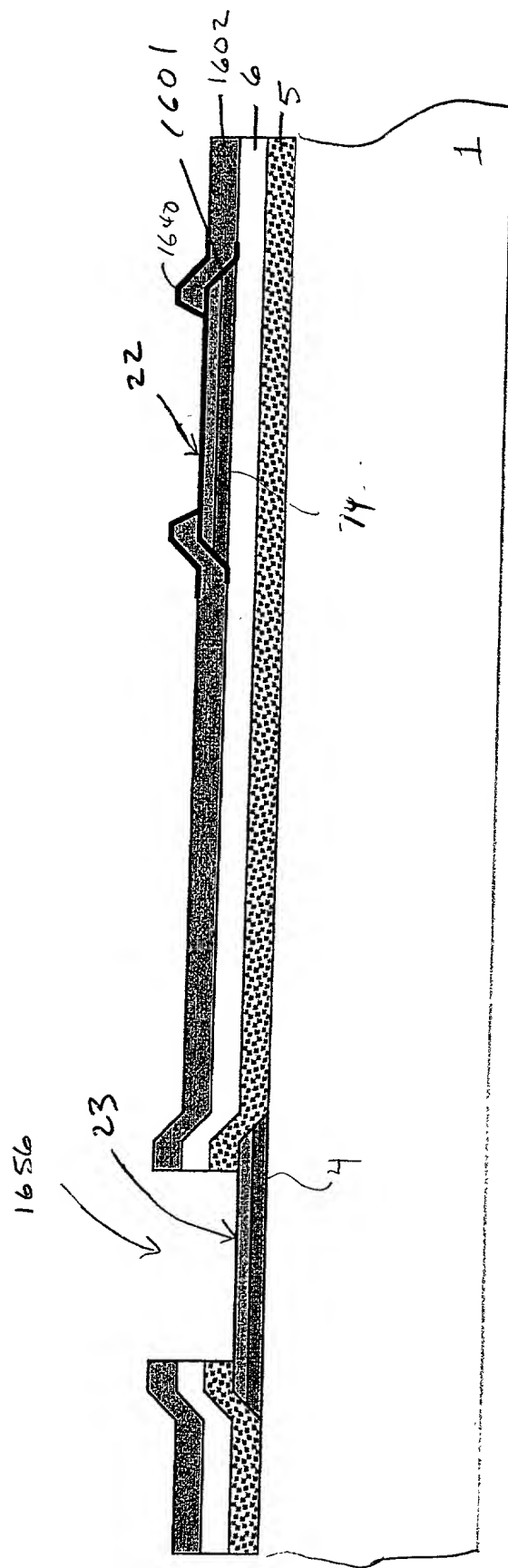


FIG 16 J

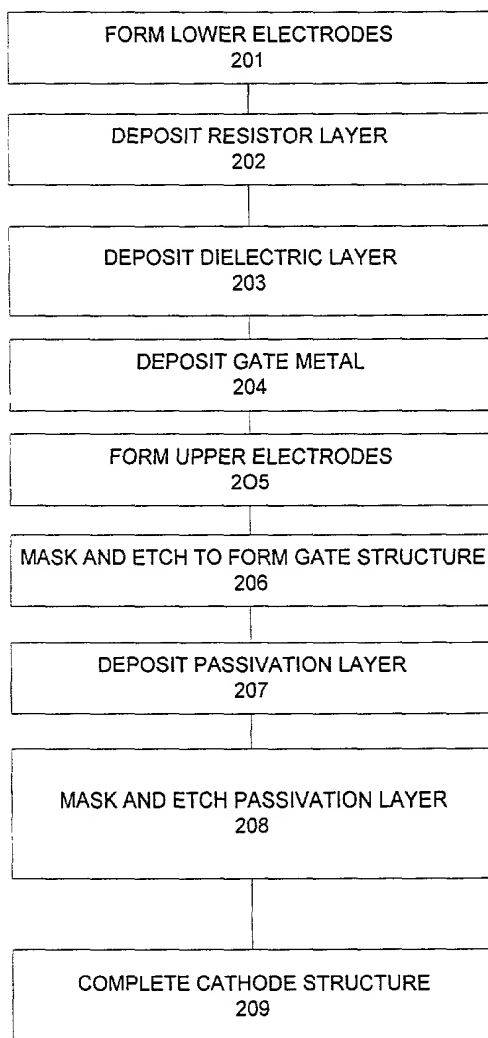


FIG. 17

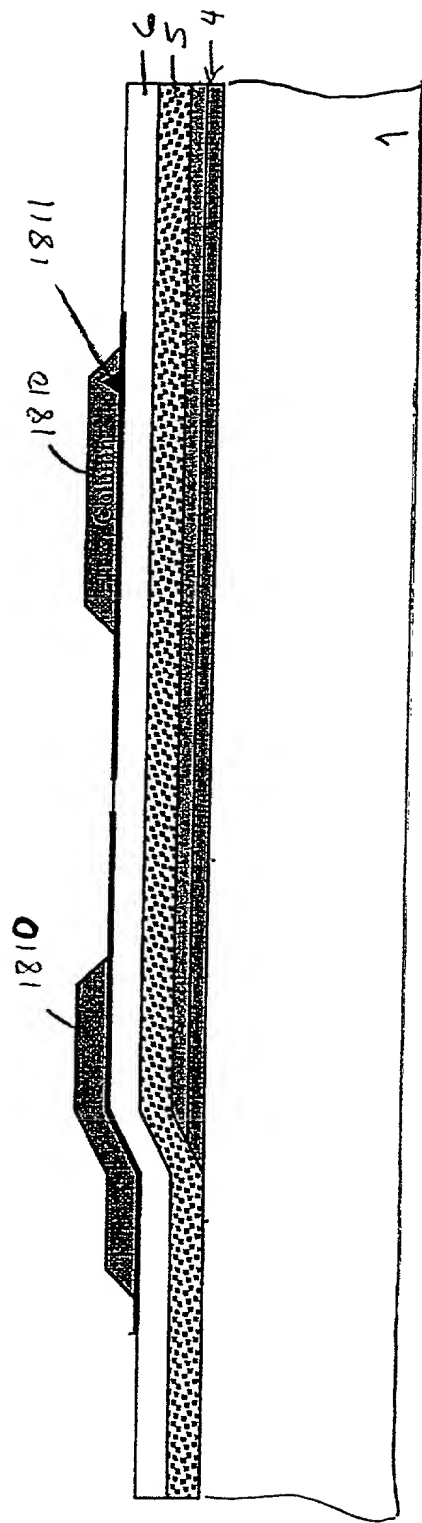


FIG. 18C

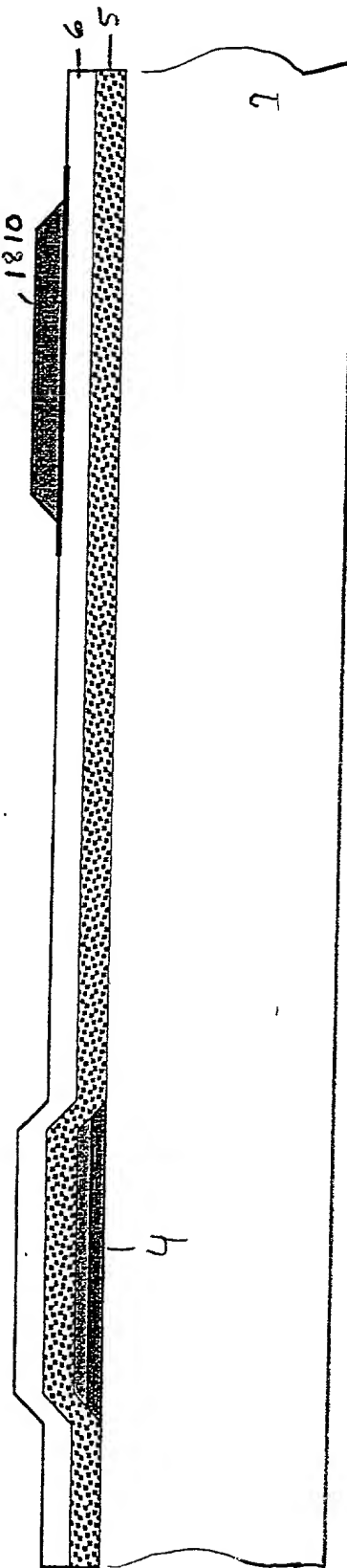
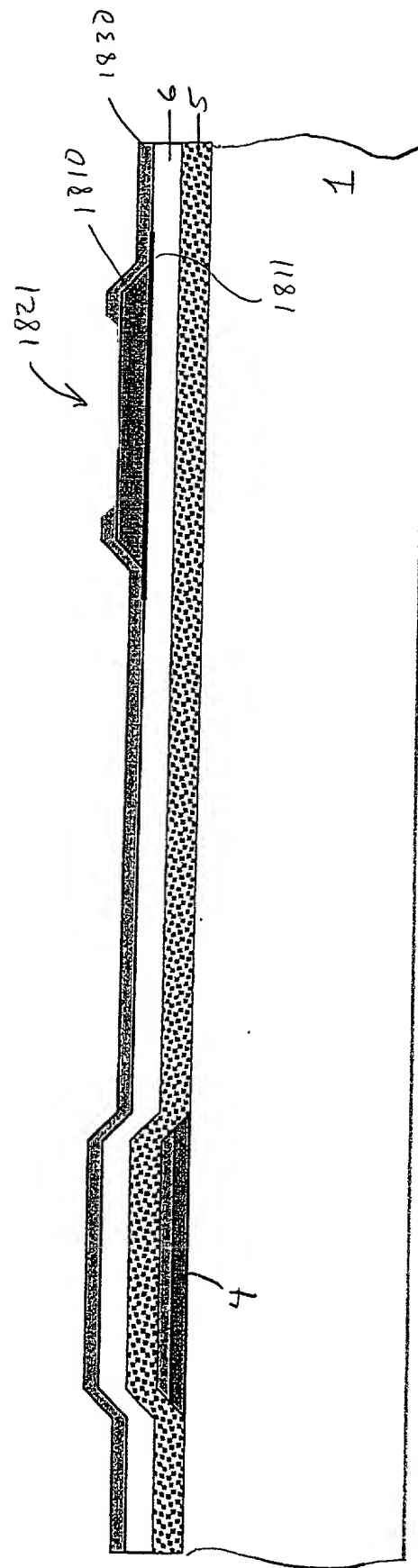
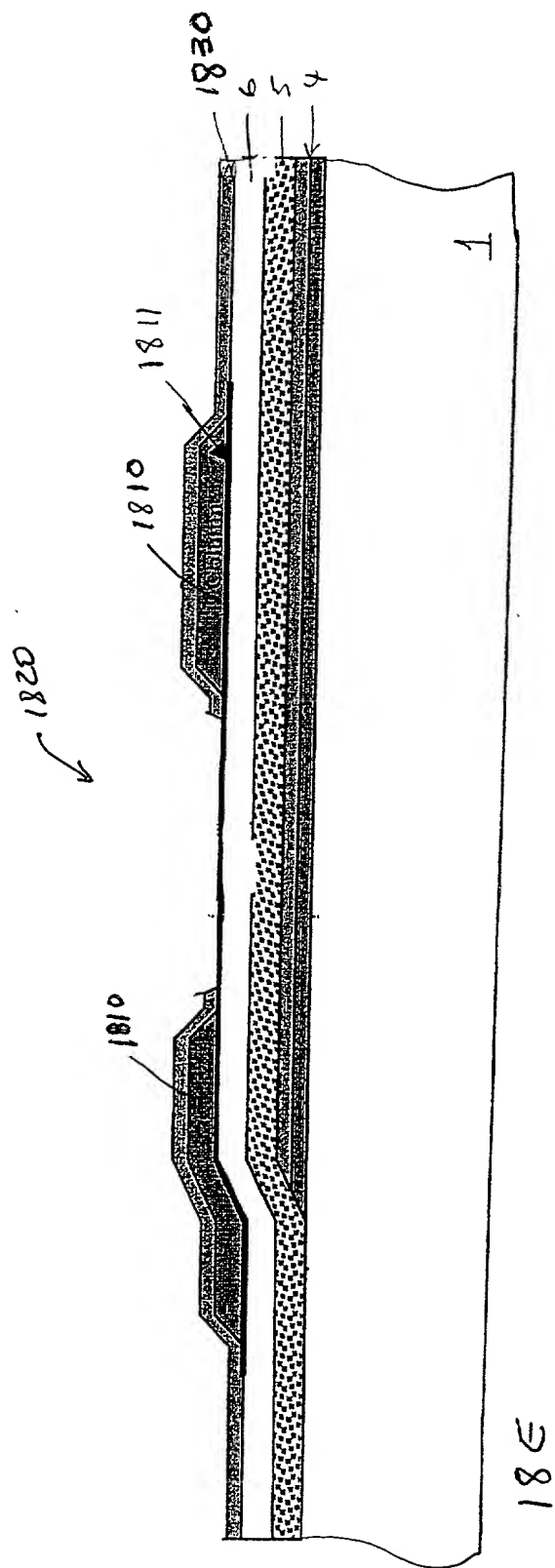


FIG. 18D.



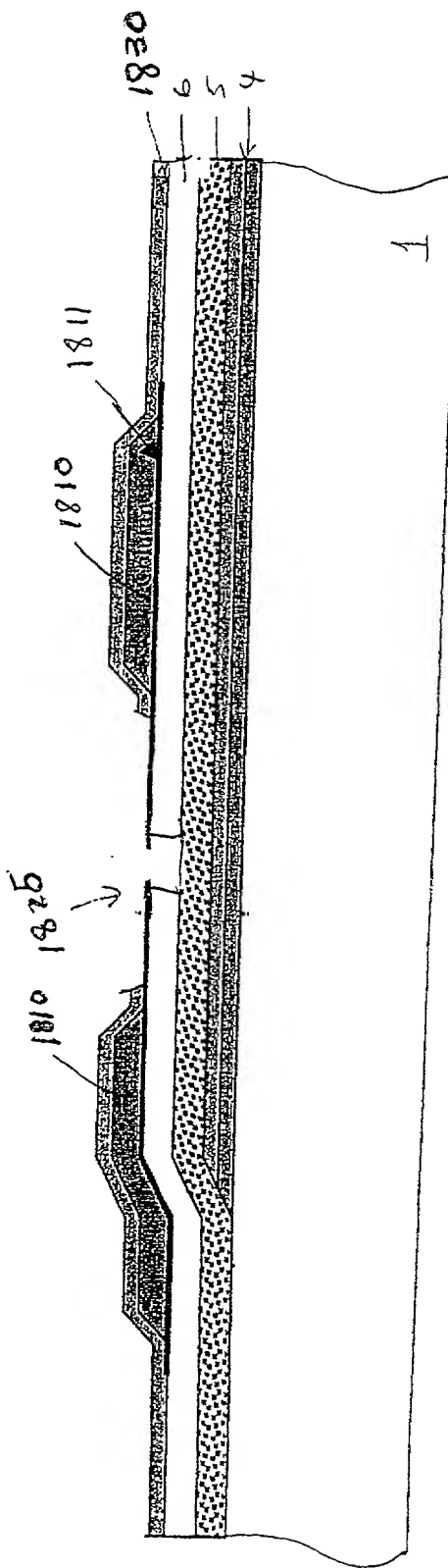


FIG. 18G

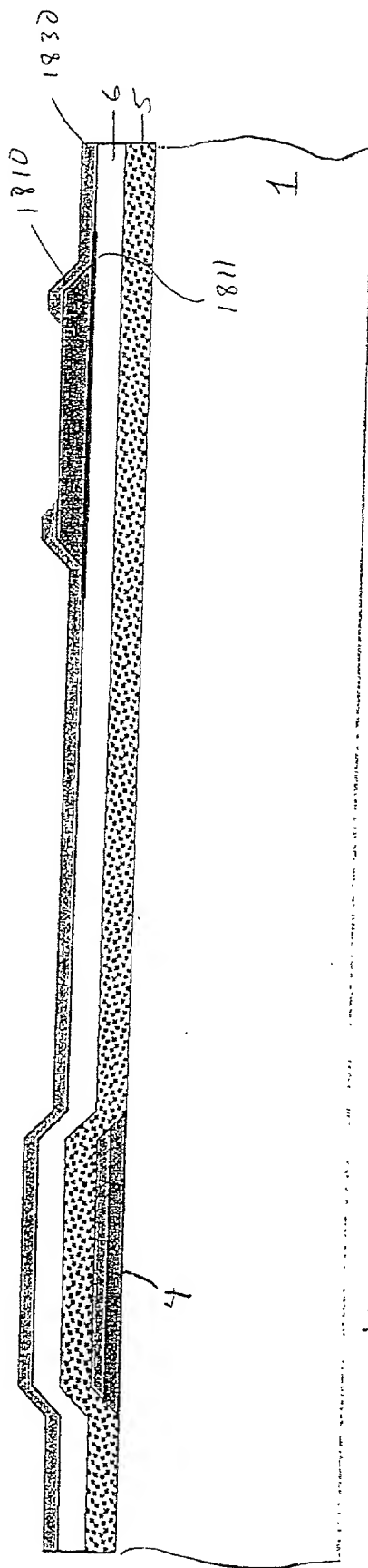


FIG. 18H

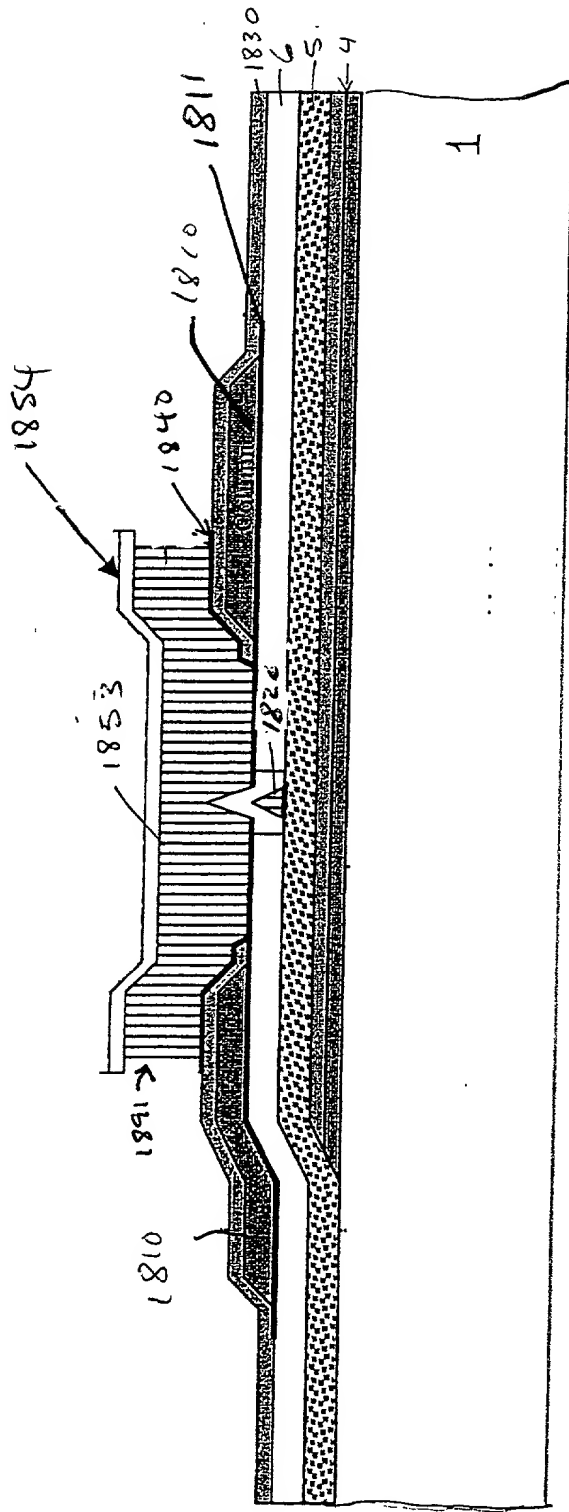


FIG 18 I

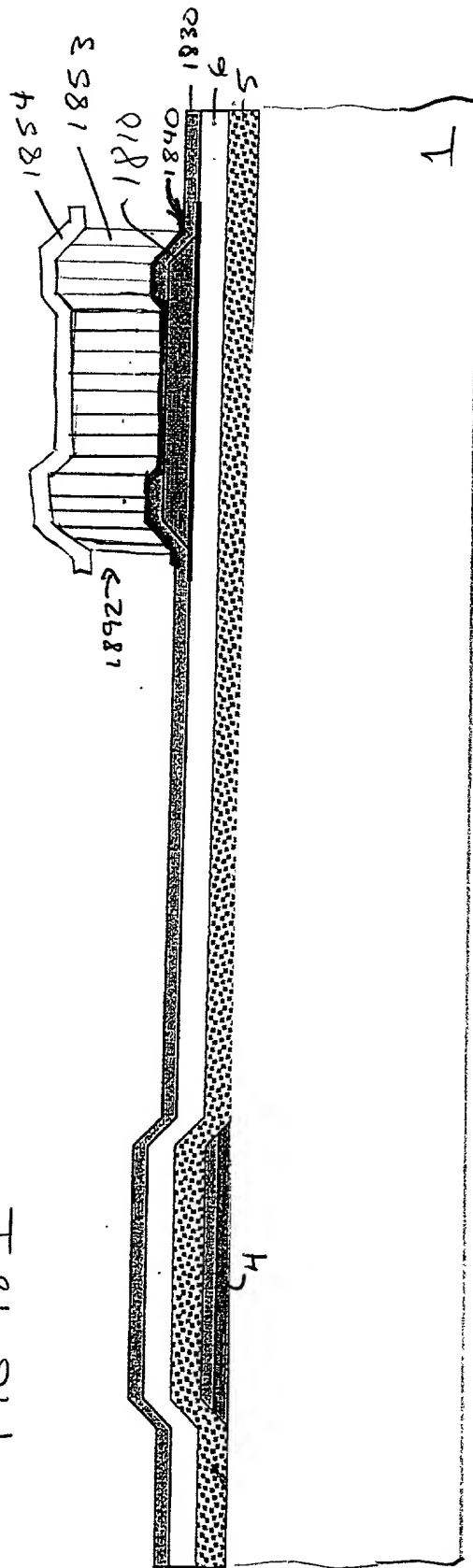


FIG 18 J

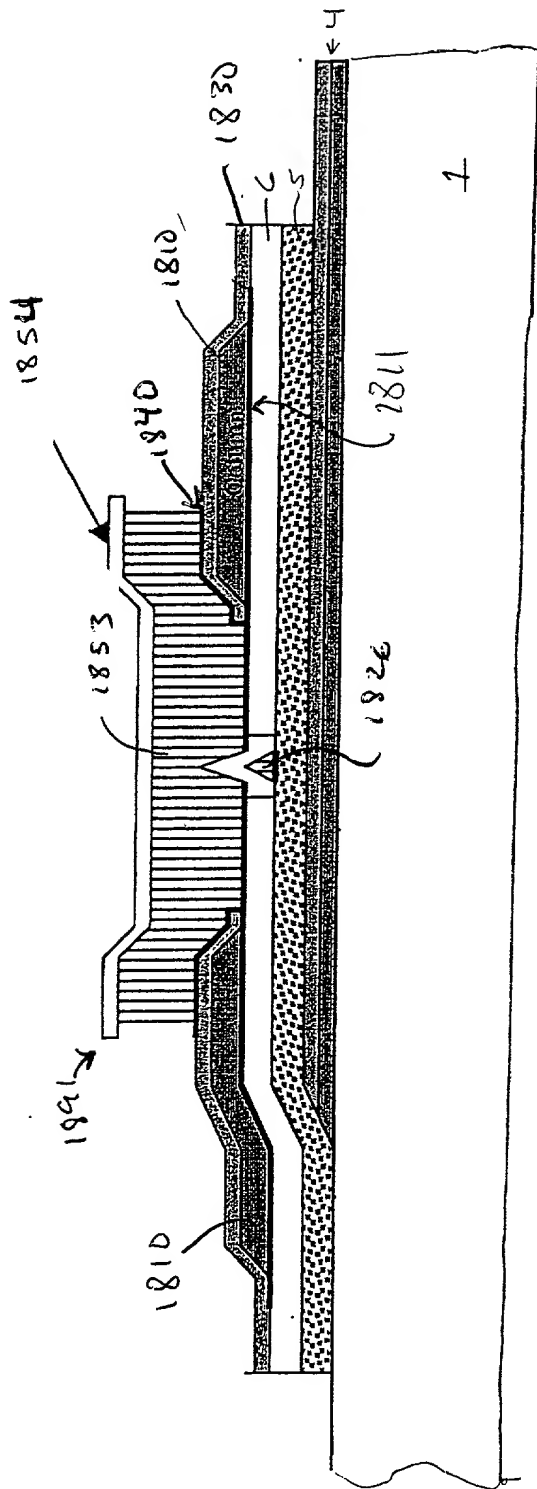


FIG 18 K

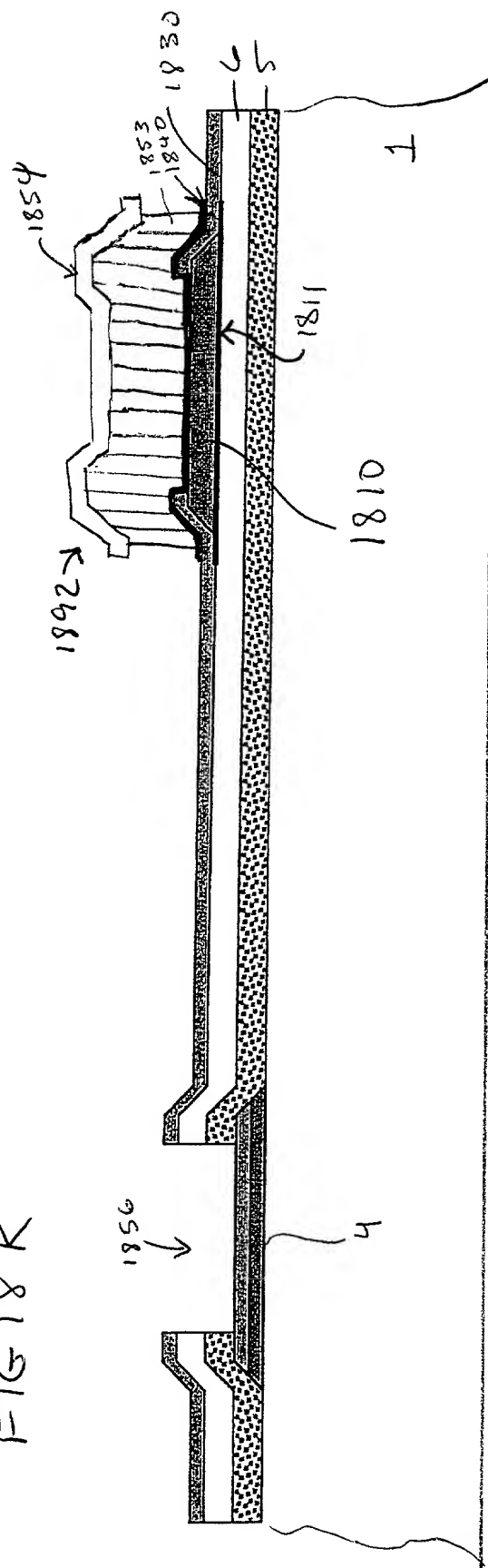


FIG 18 L

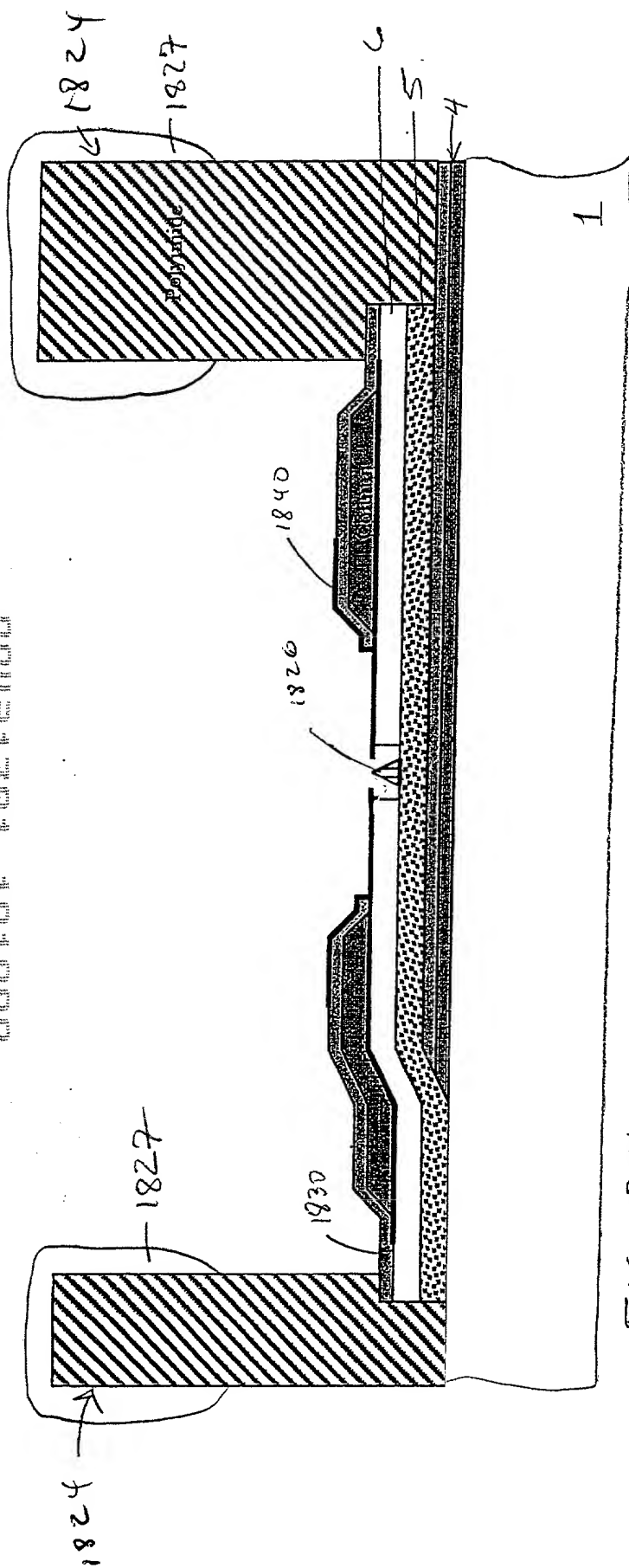
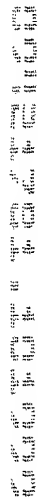


FIG-18M

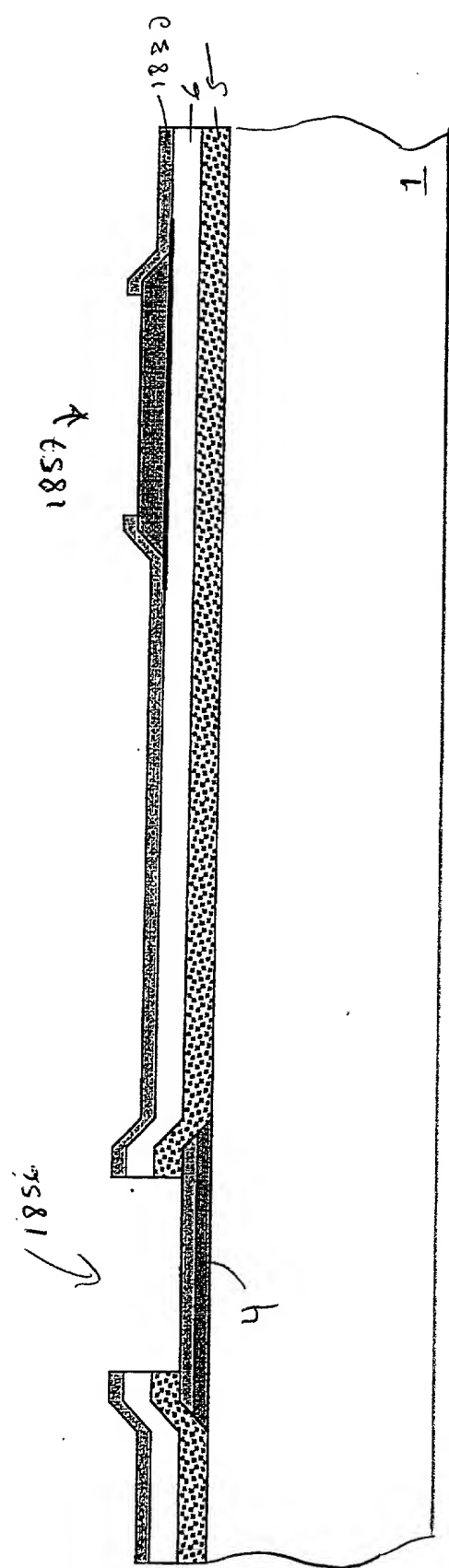


FIG 1822

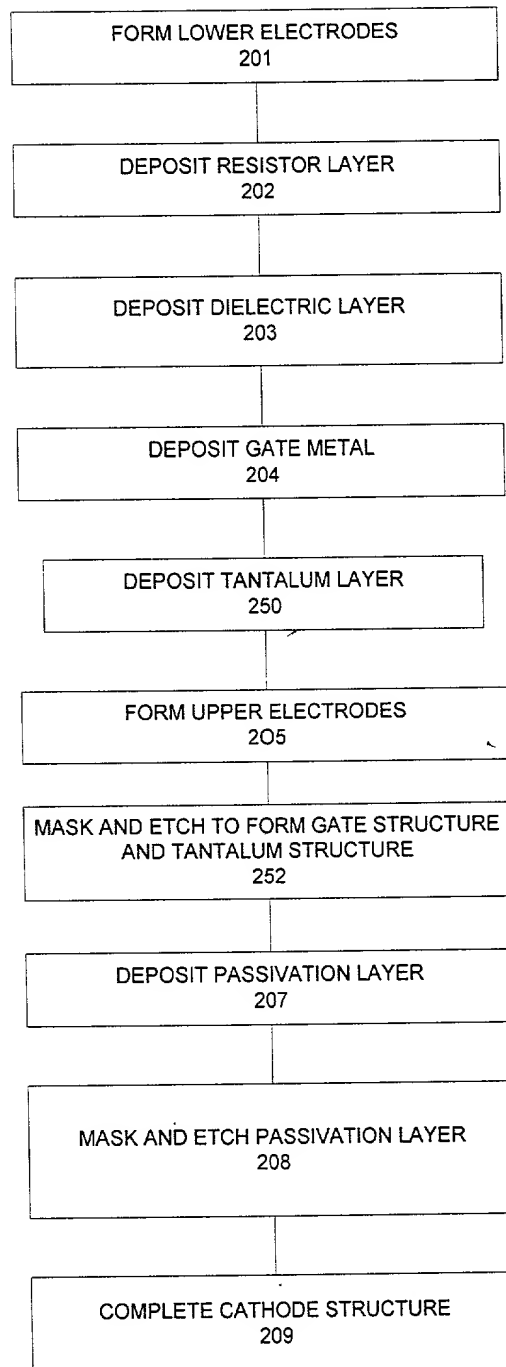


FIG. 19

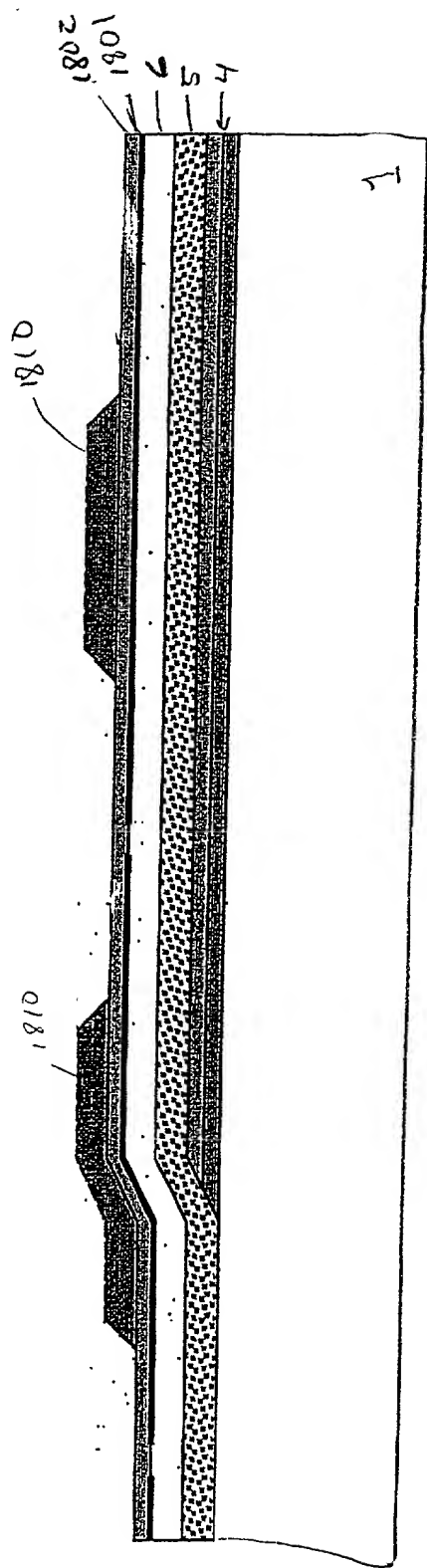


FIG. 20A

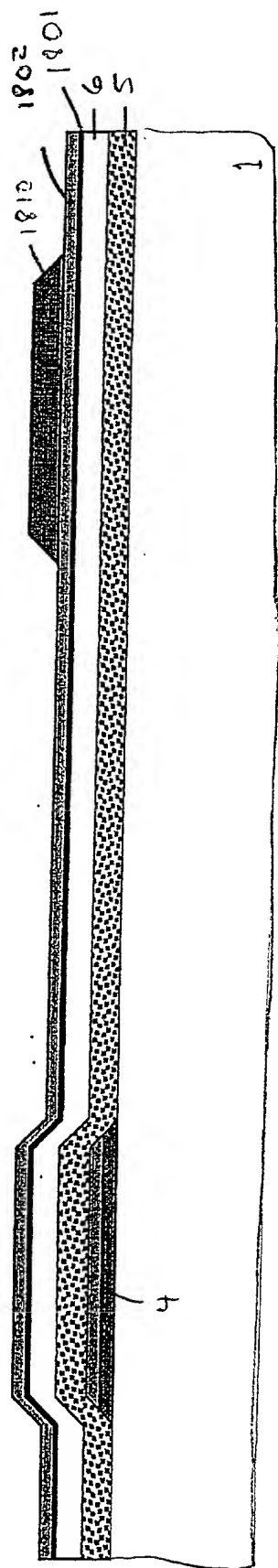


FIG. 20B

FIG. 20C

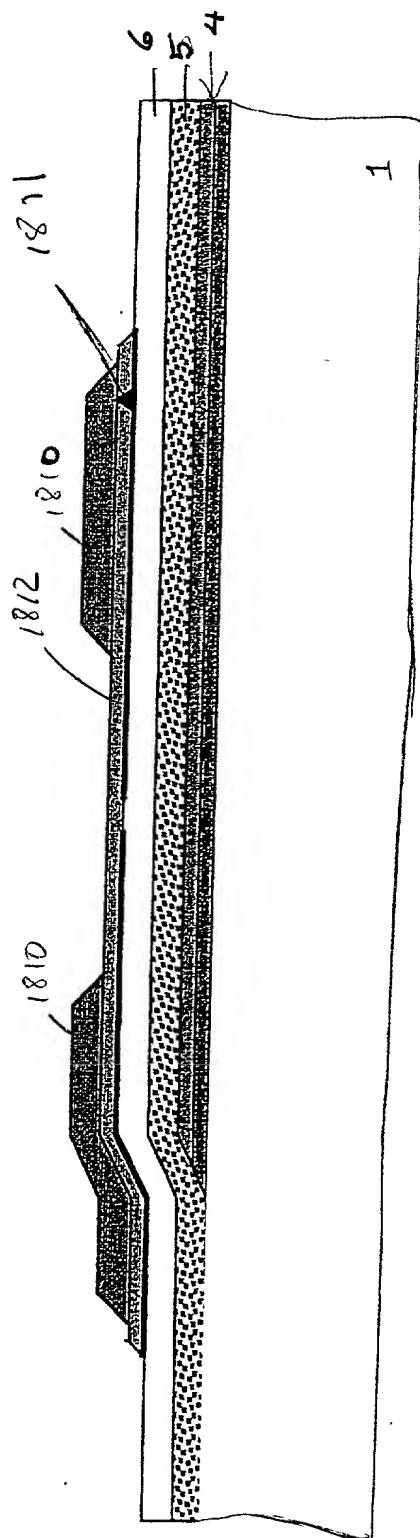


FIG. 20C

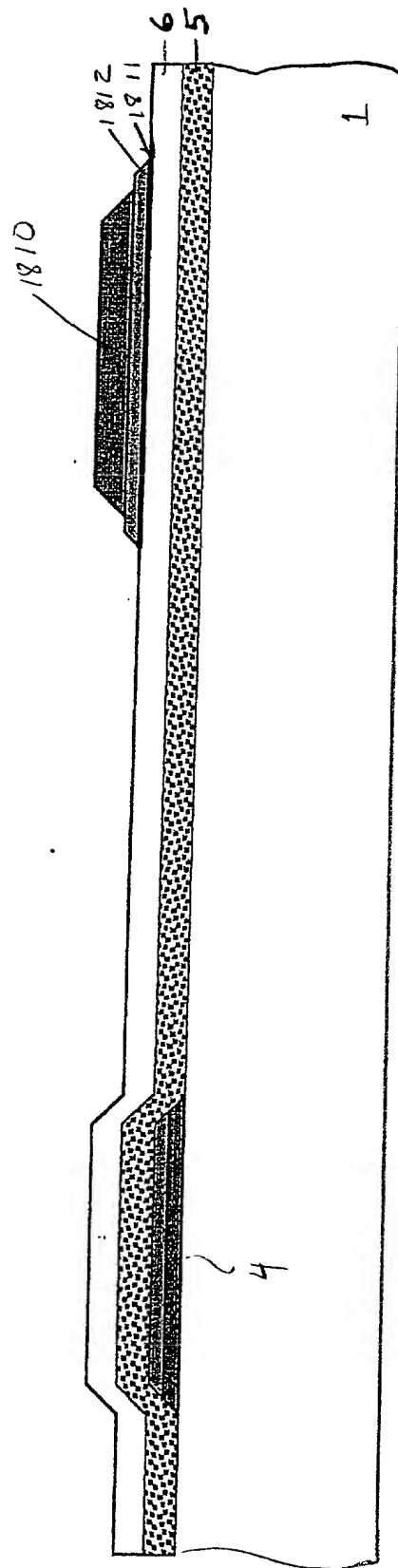


FIG. 20D

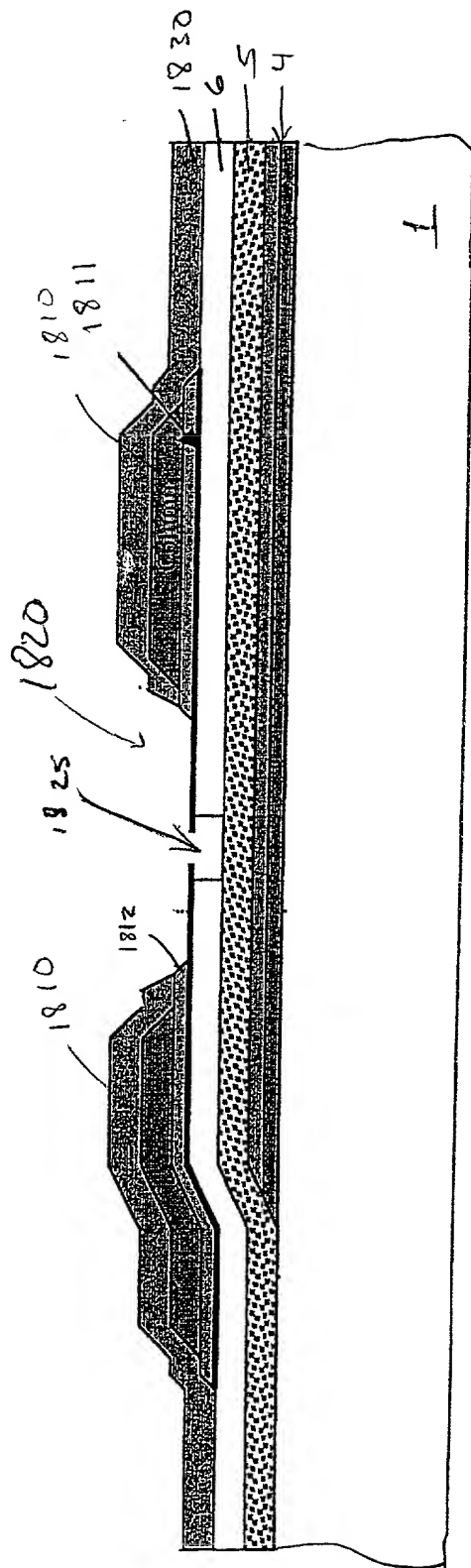


FIG 20E

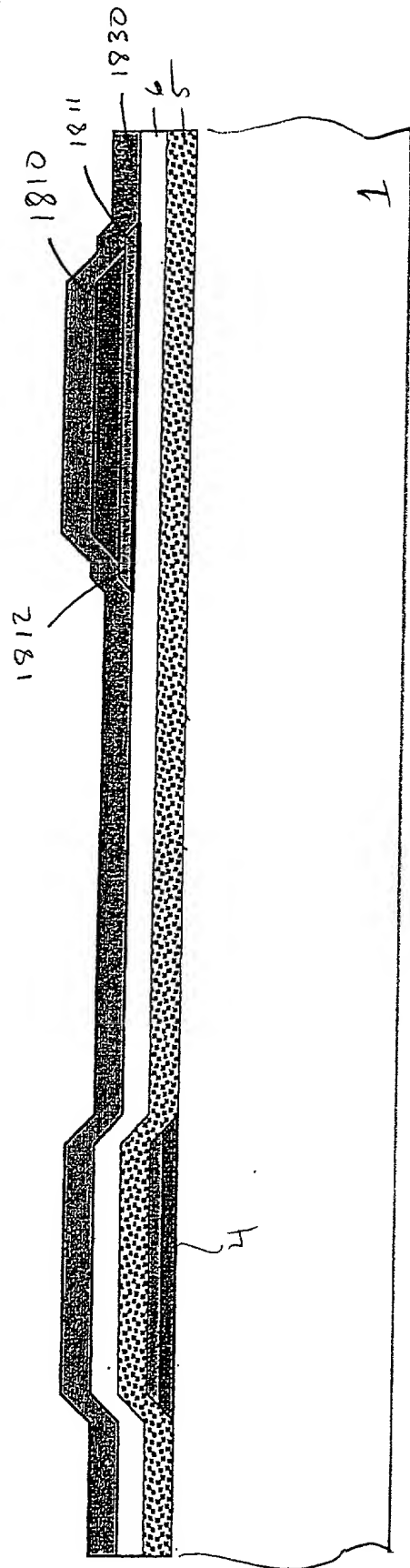


FIG 20F

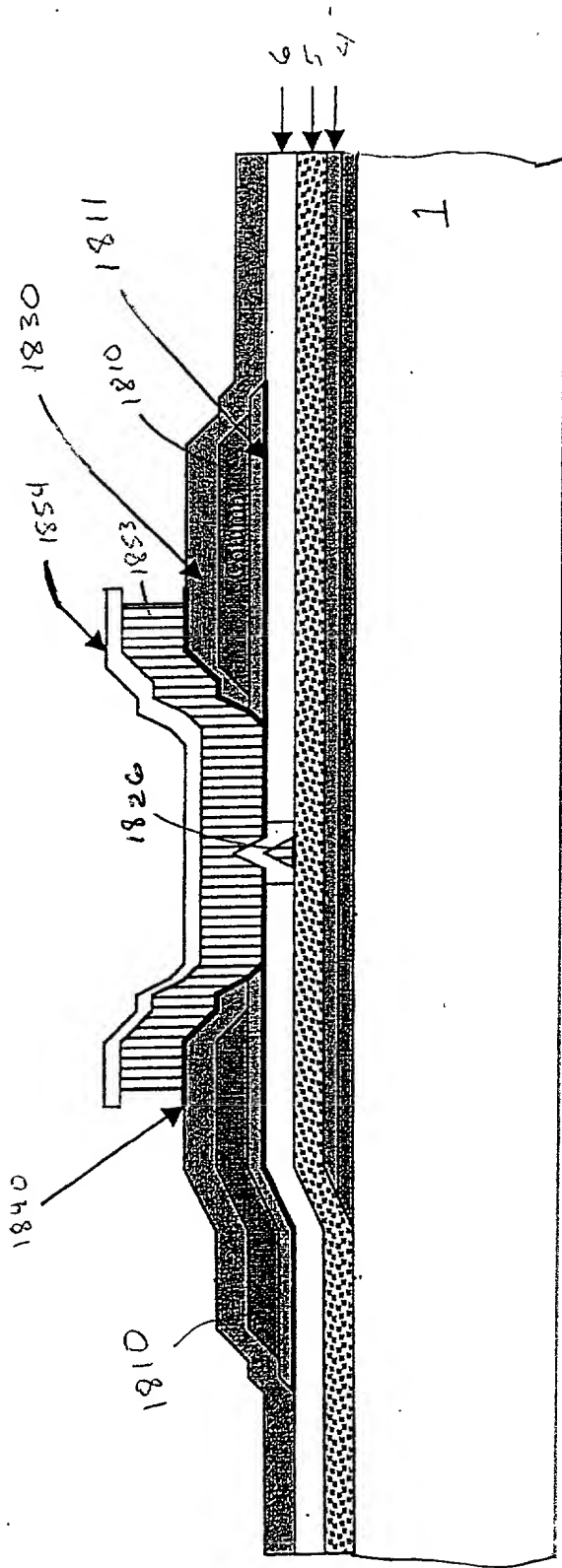


FIG. 20G

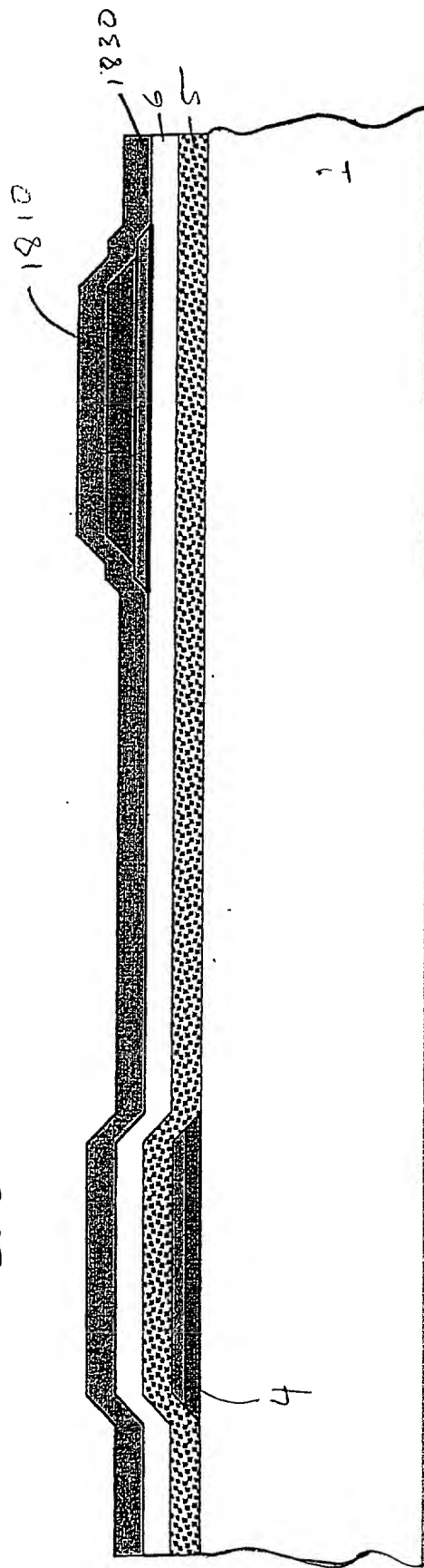


FIG. 20H

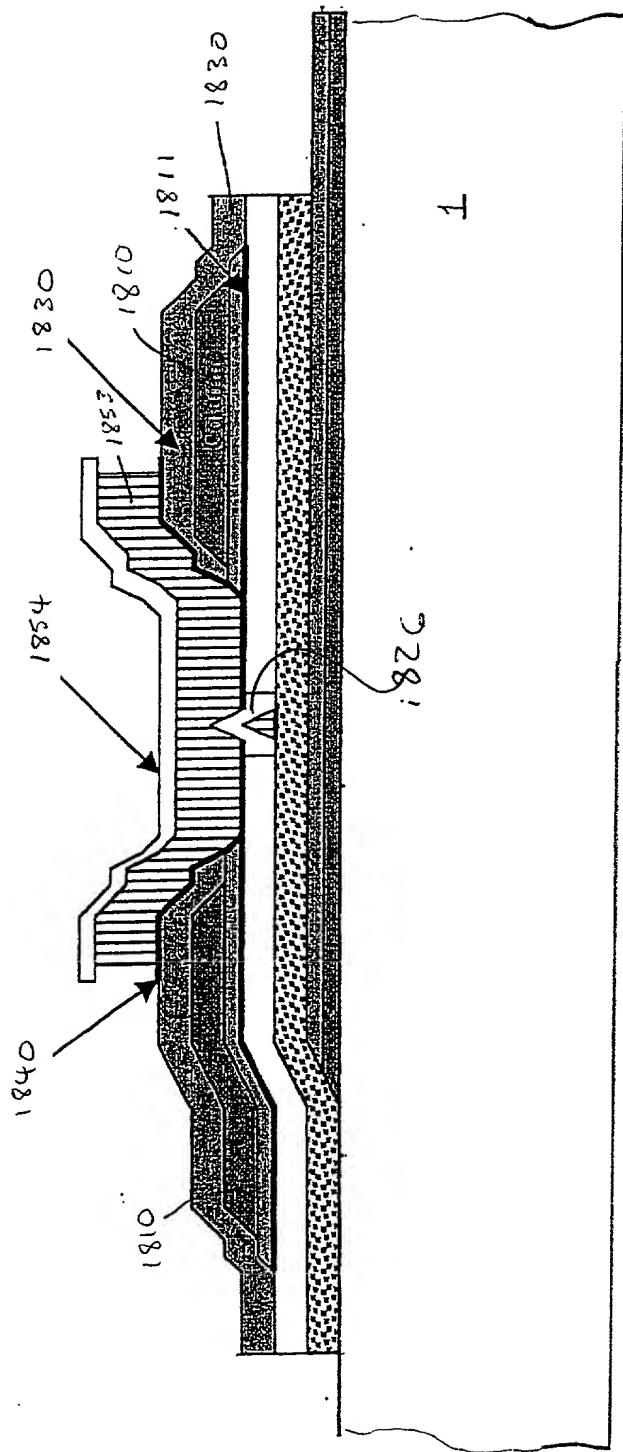


FIG. 20I

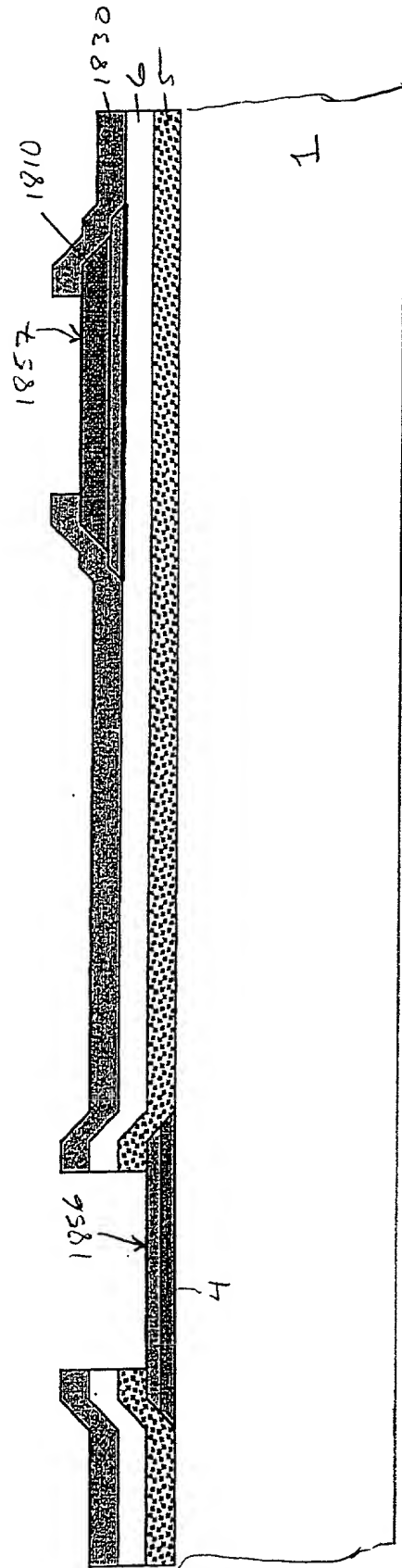
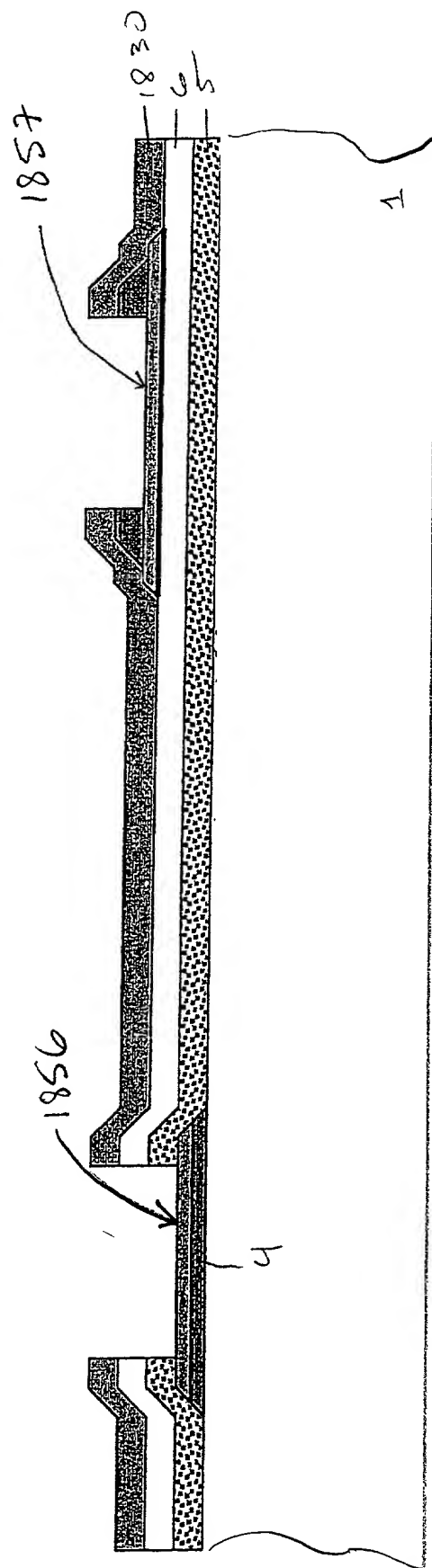
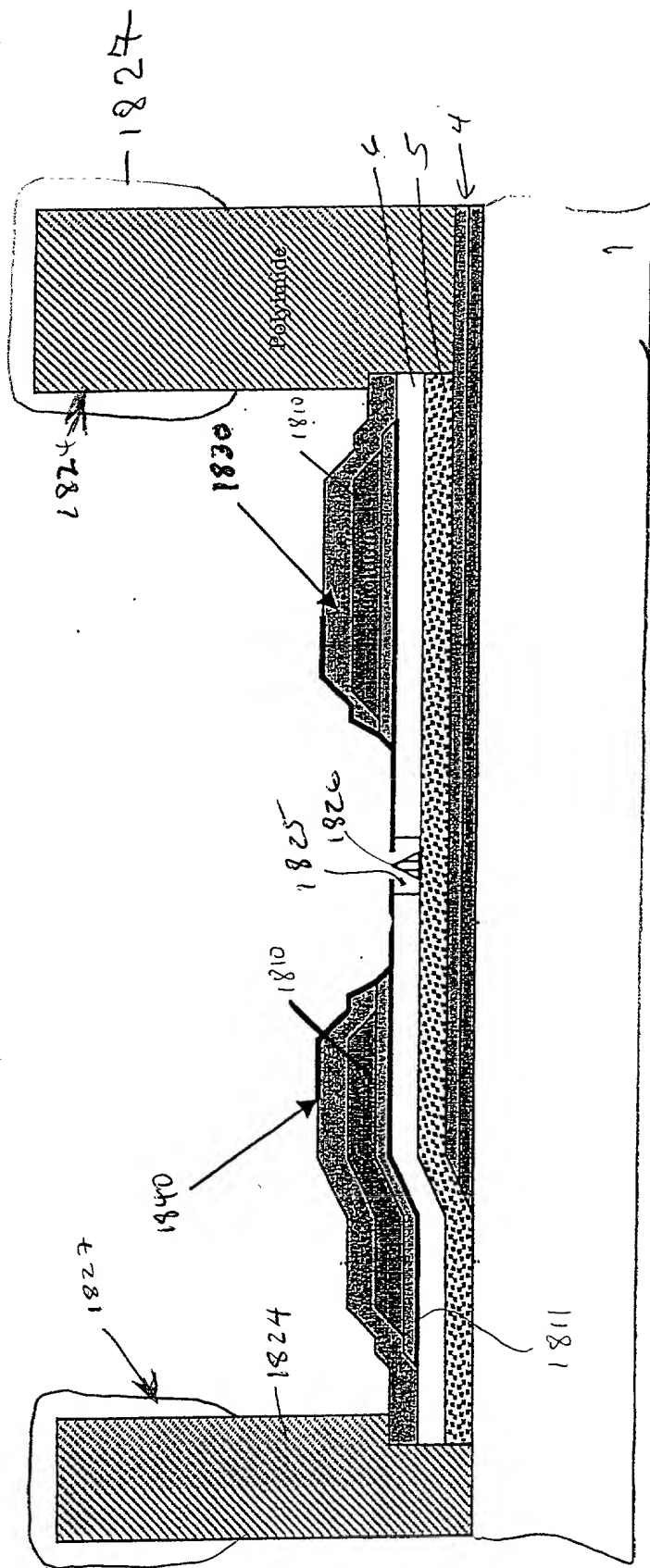


FIG. 20J



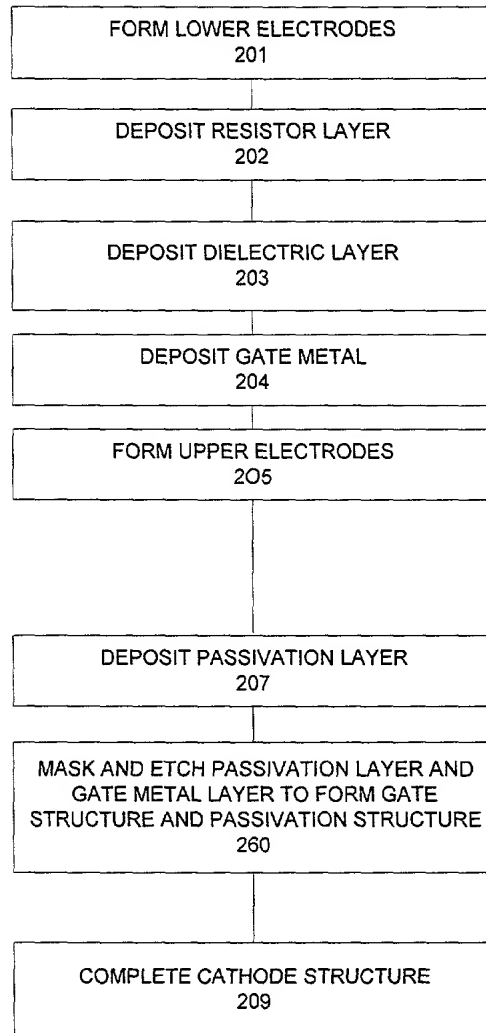


FIG. 21

FIG. 22A

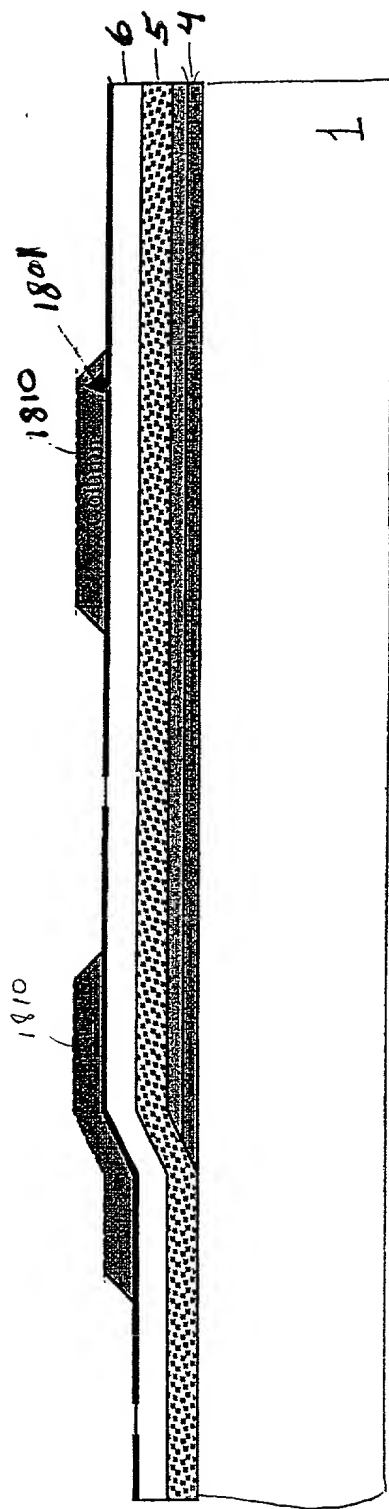
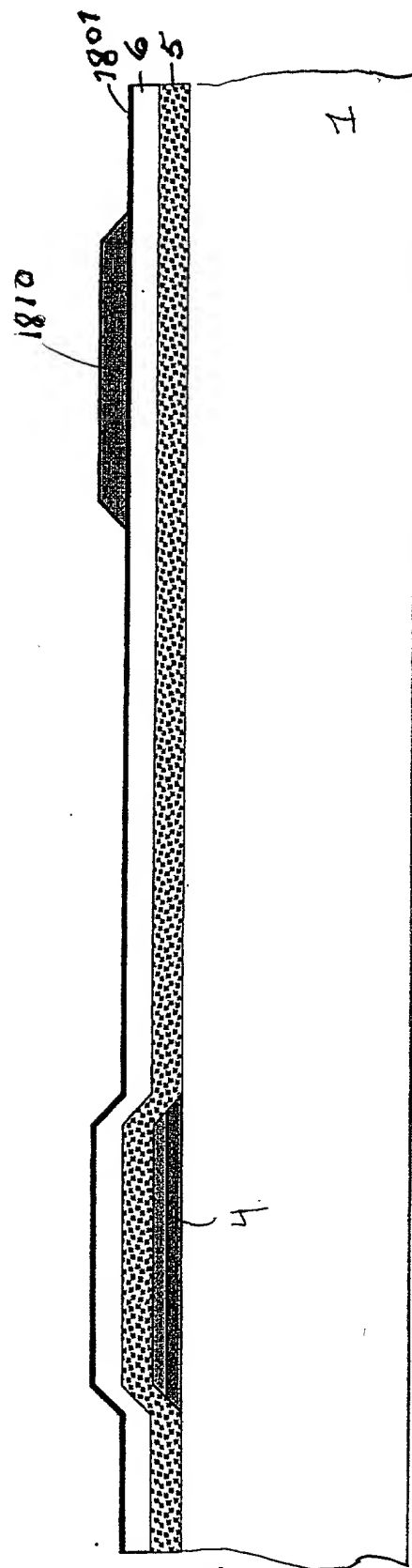


FIG. 22B



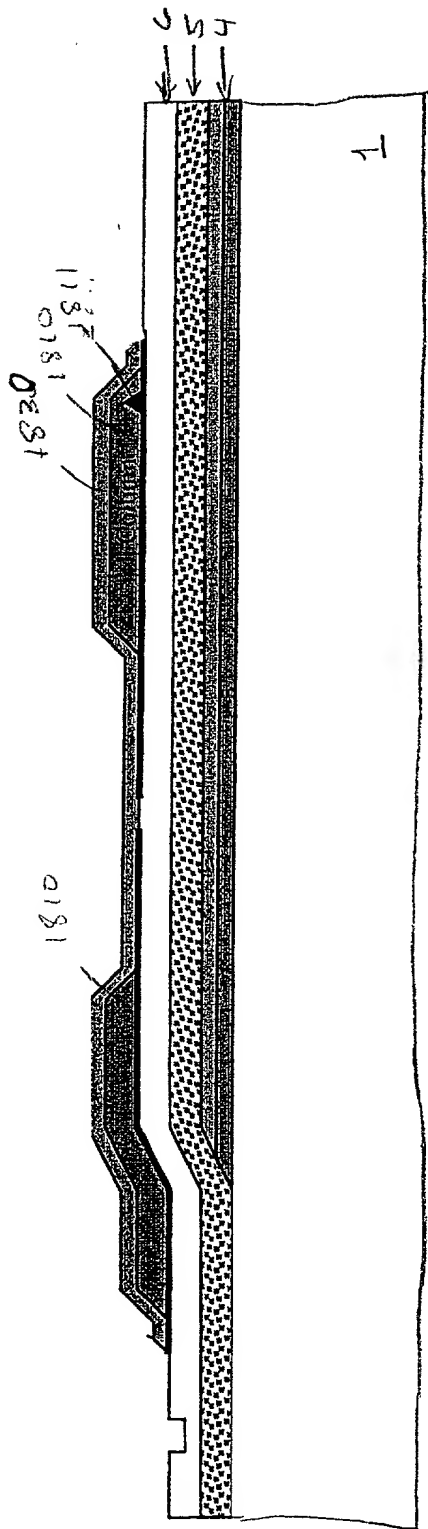


FIG. 22C

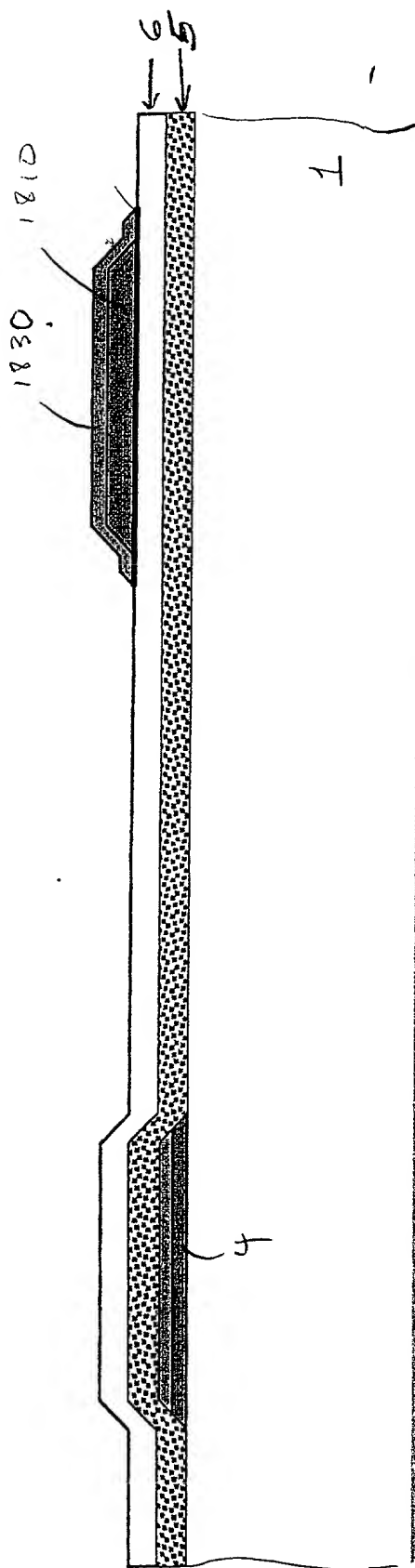


FIG. 22D

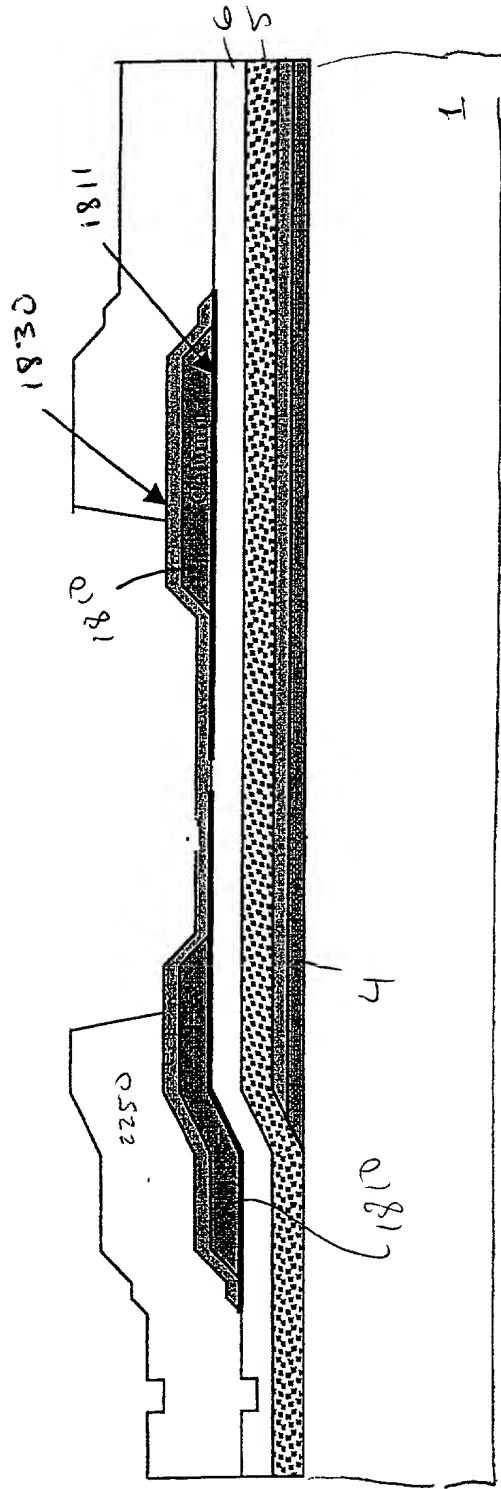


FIG 22E

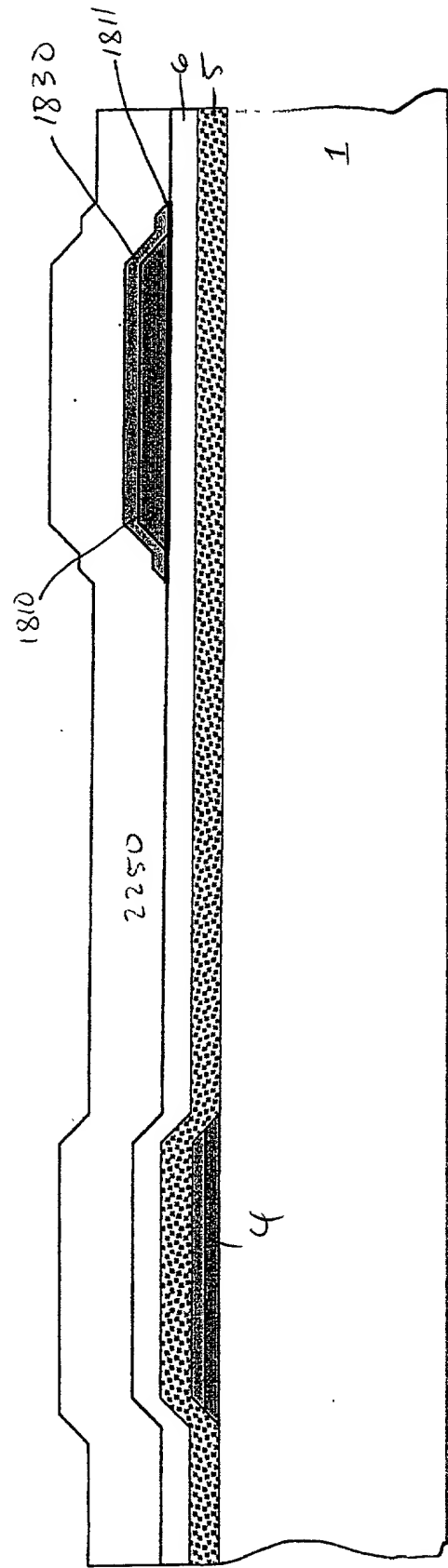
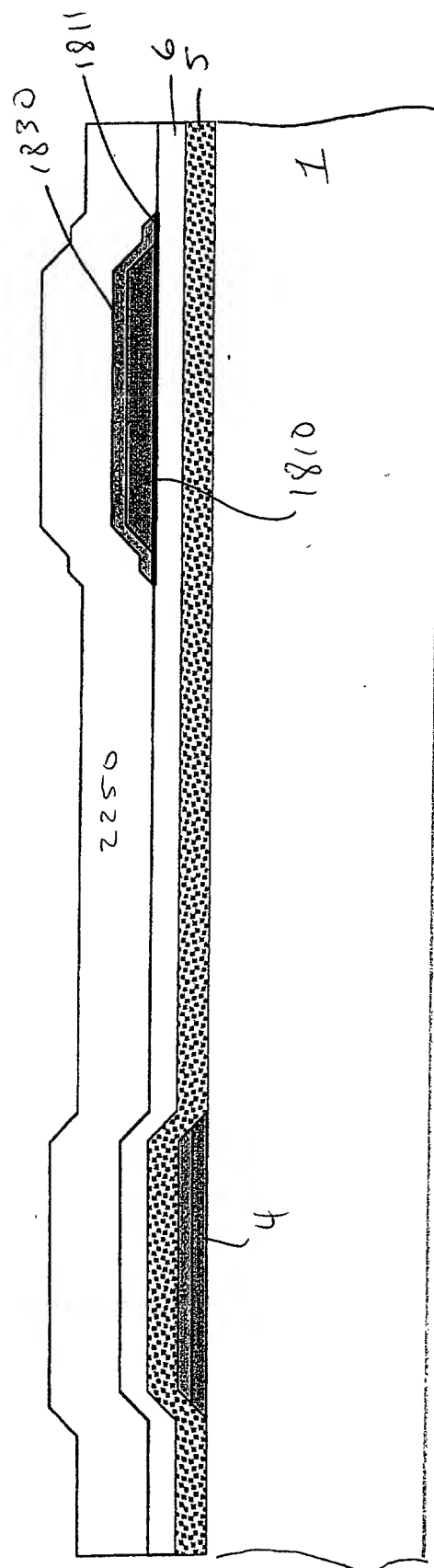
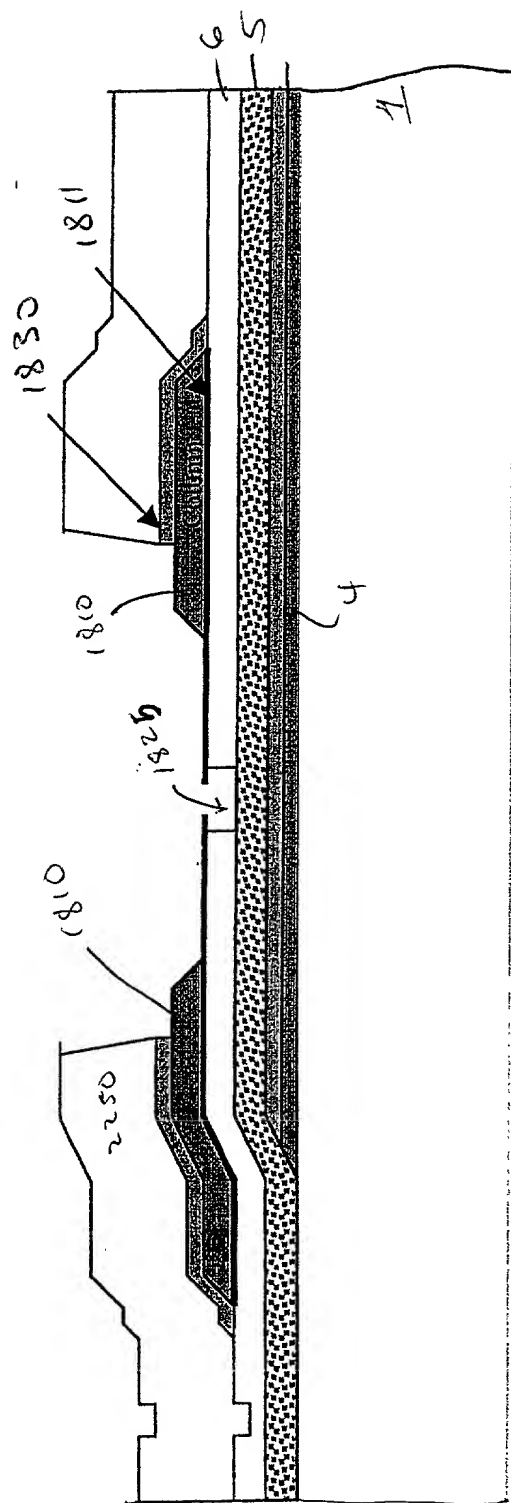


FIG 22F



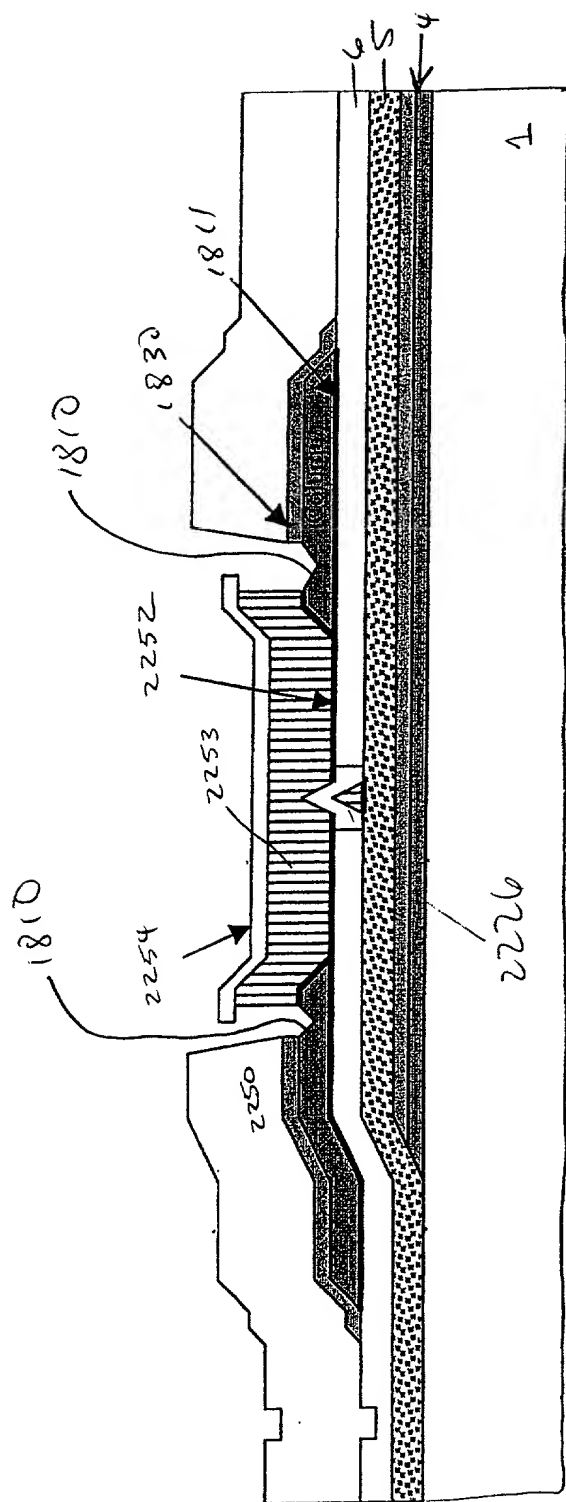
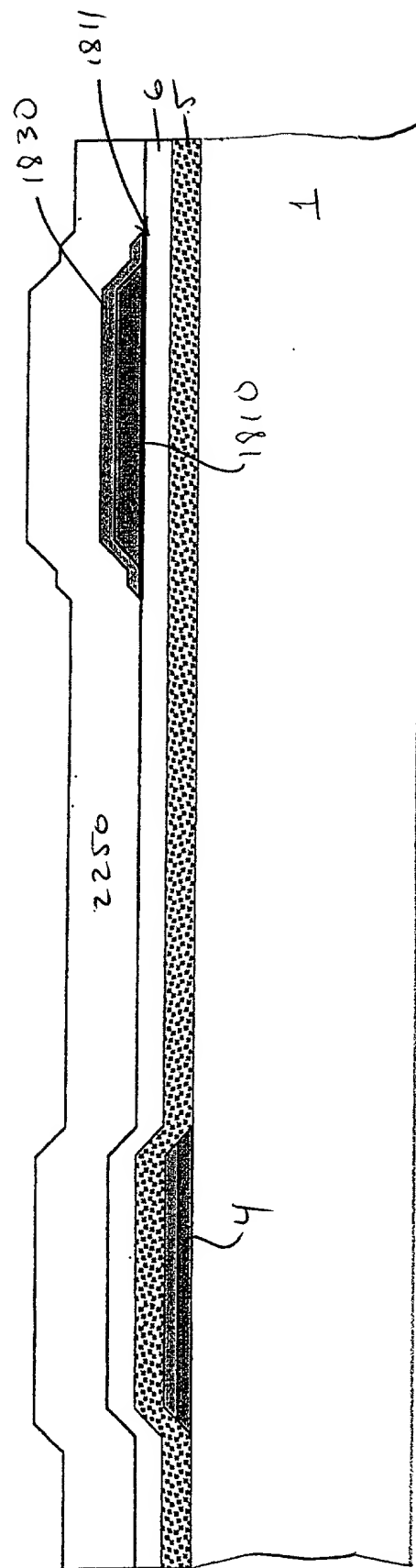
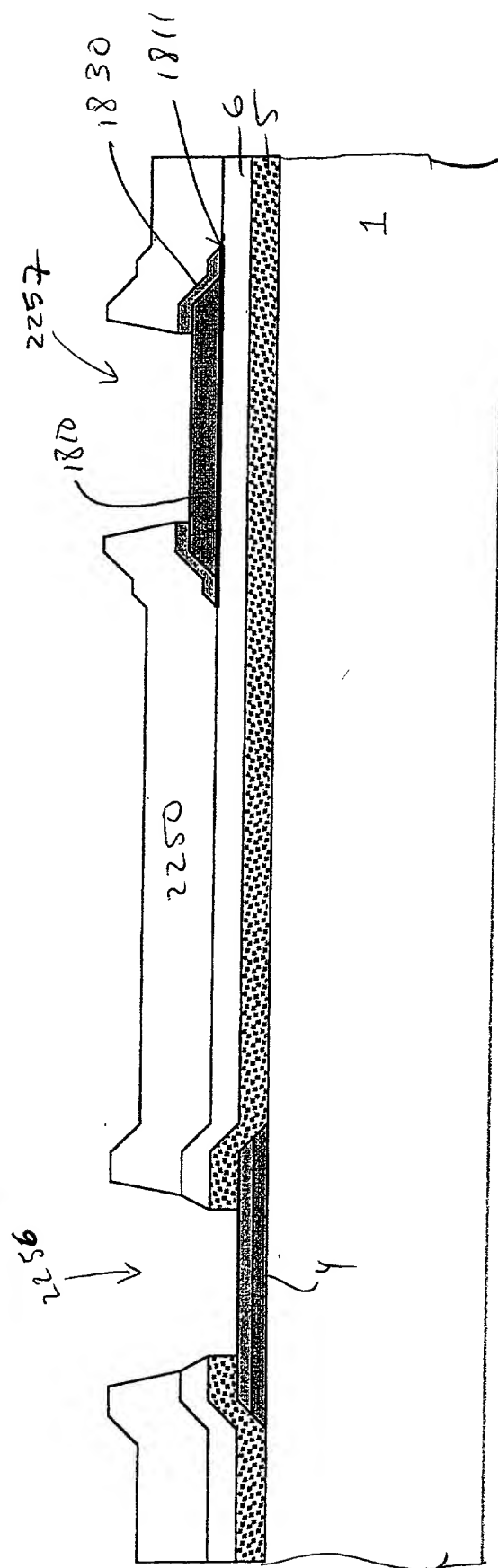
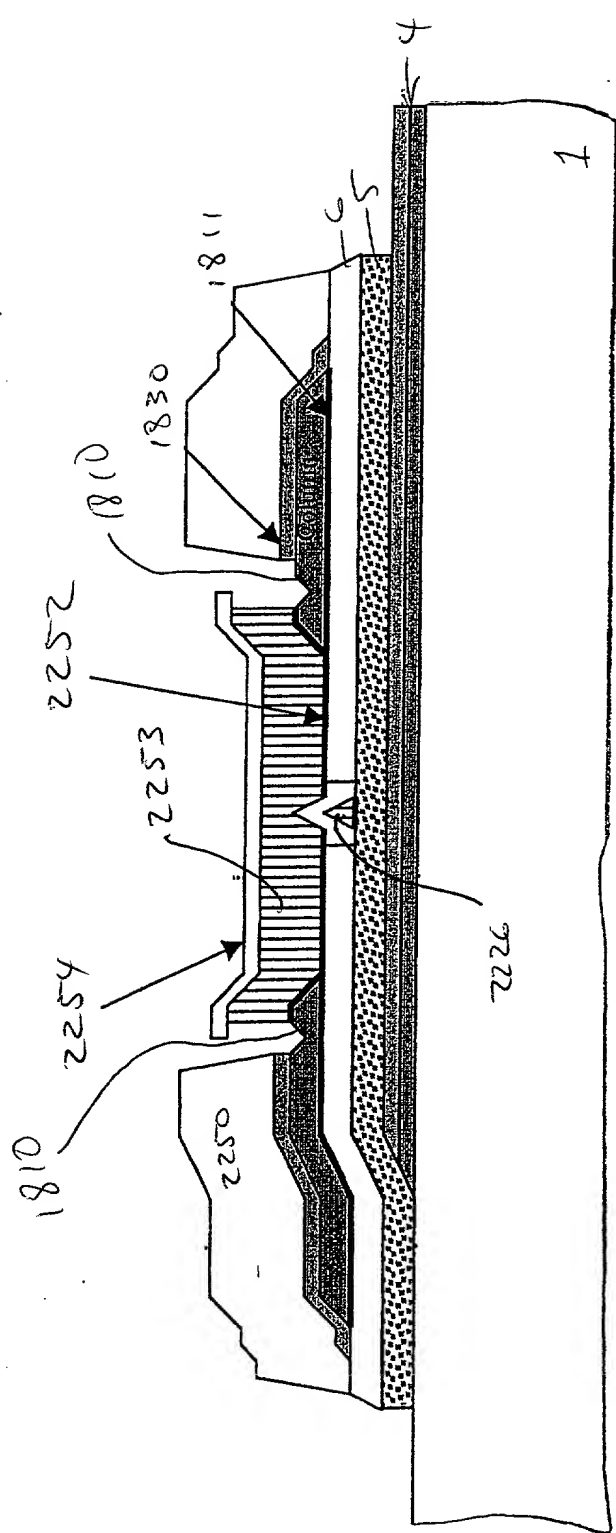
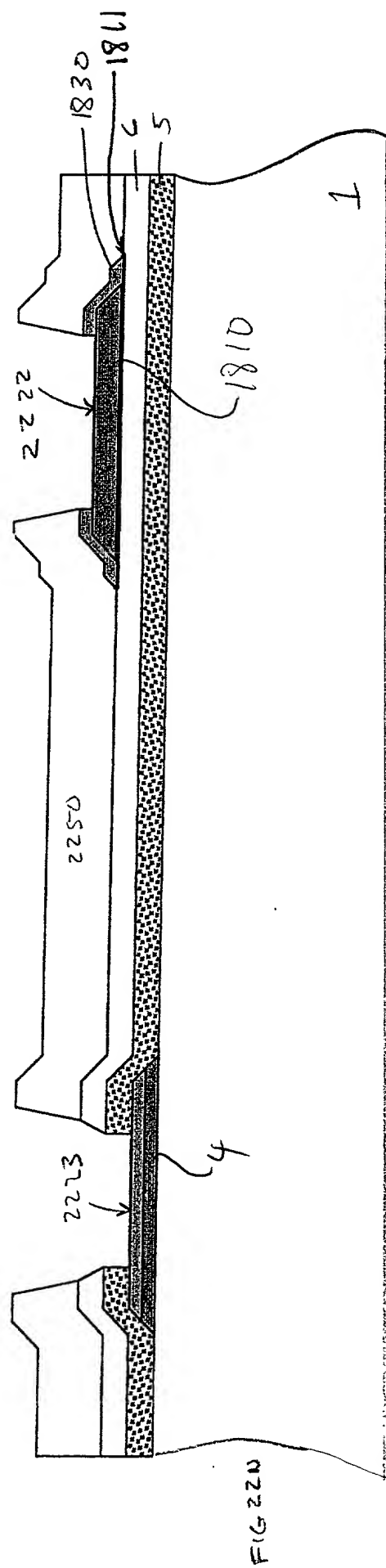
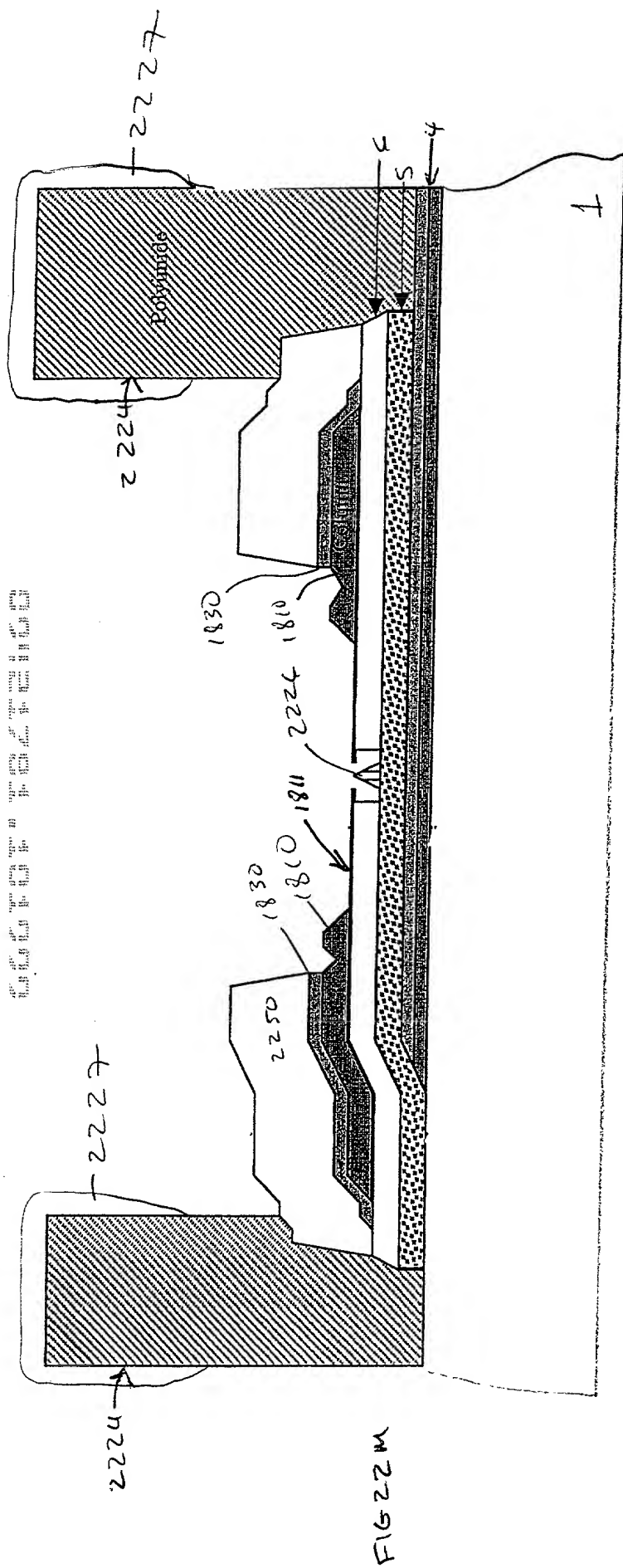


FIG. 22I



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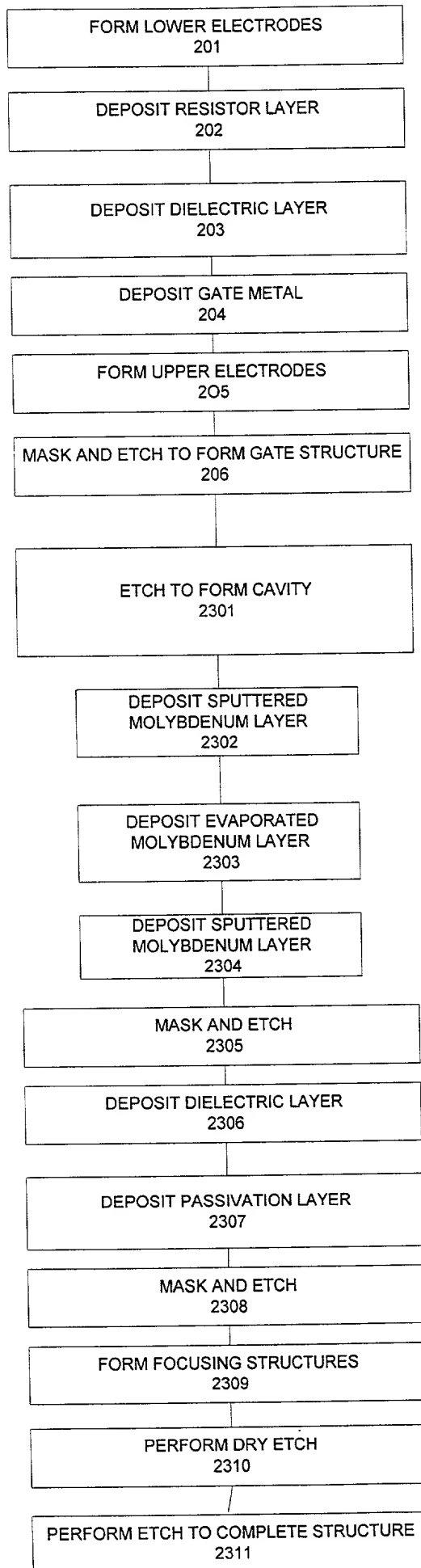


FIG. 23

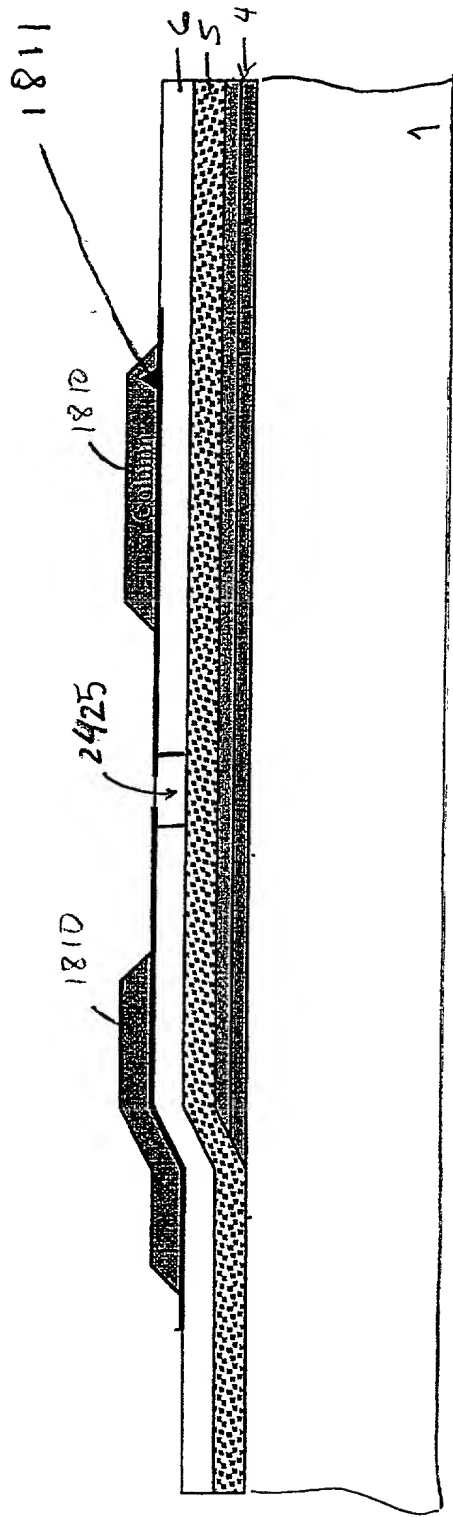


FIG. 24A

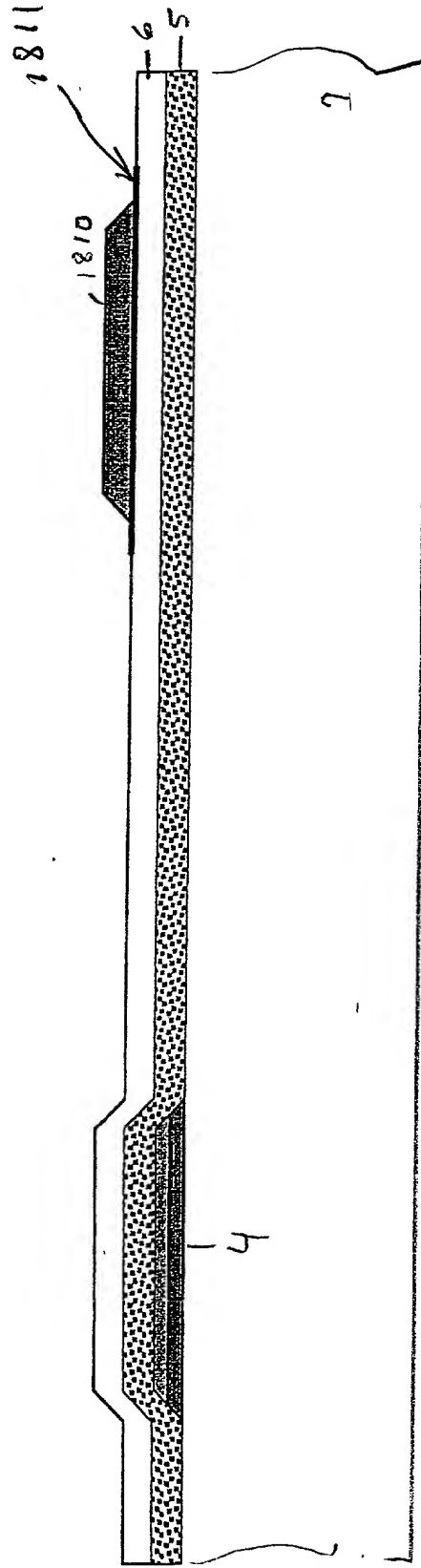


FIG. 24B

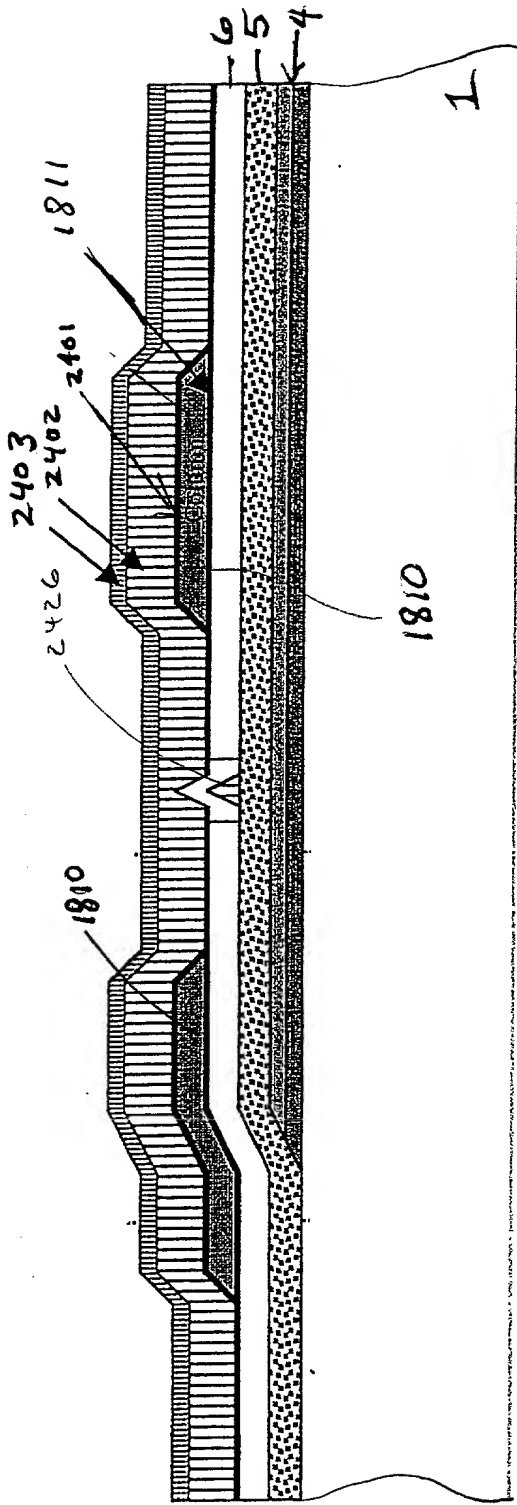


FIG. 24C

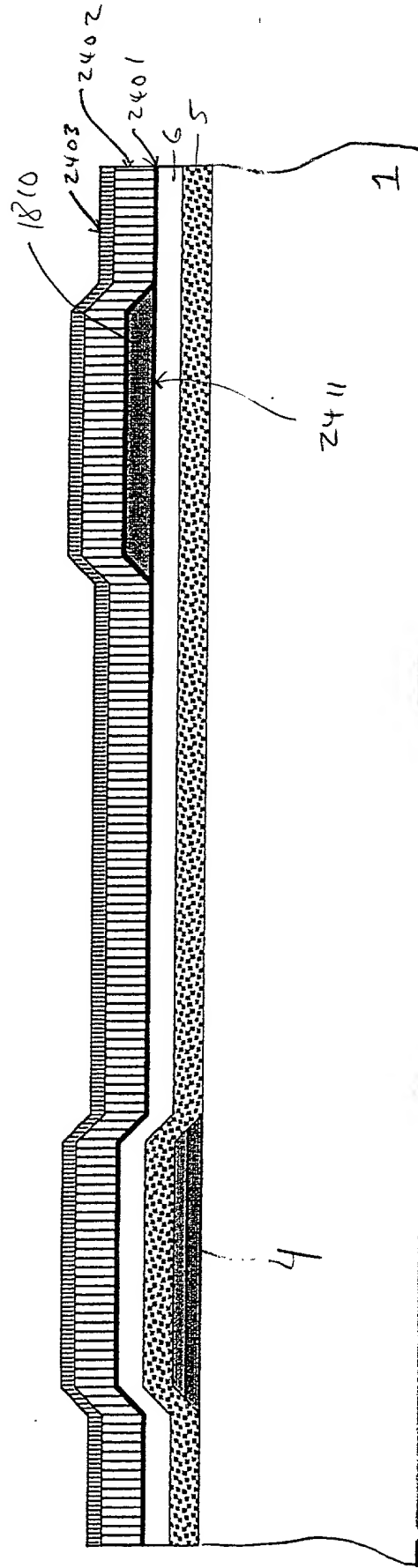


FIG. 24D

[illegible]

FIG. 24G is a cross-sectional view of a semiconductor device in a second state, after a second layer of material has been deposited over the first layer of material.

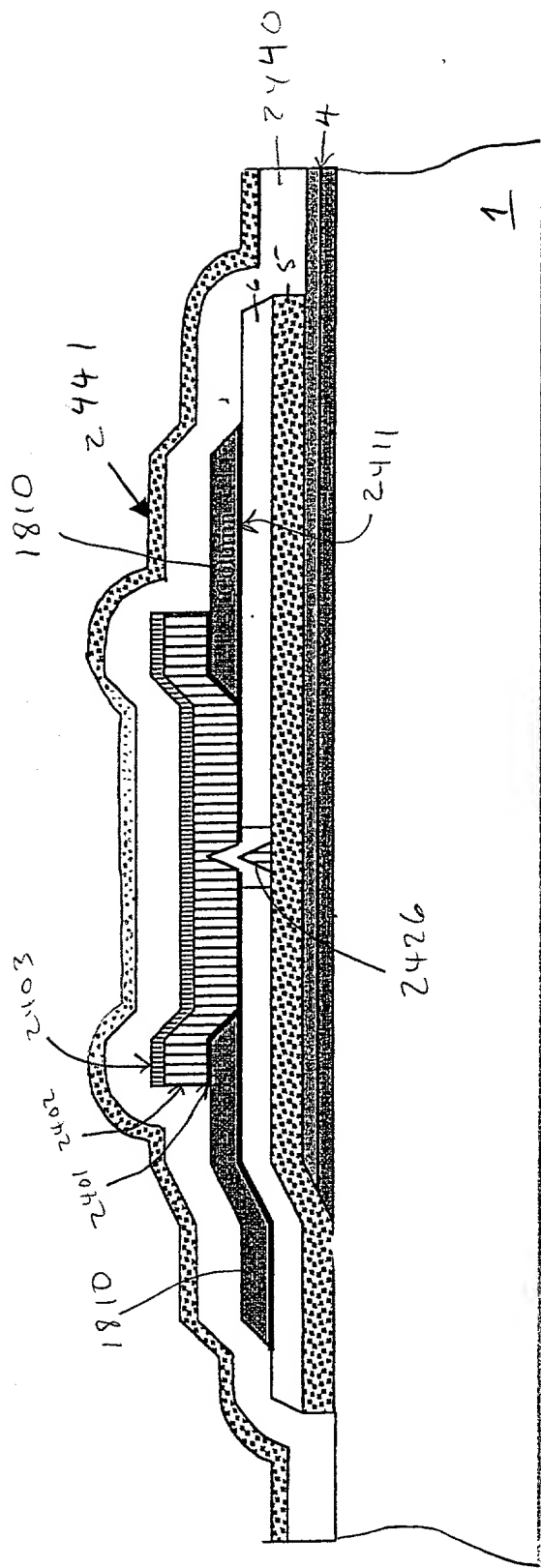


FIG. 24G

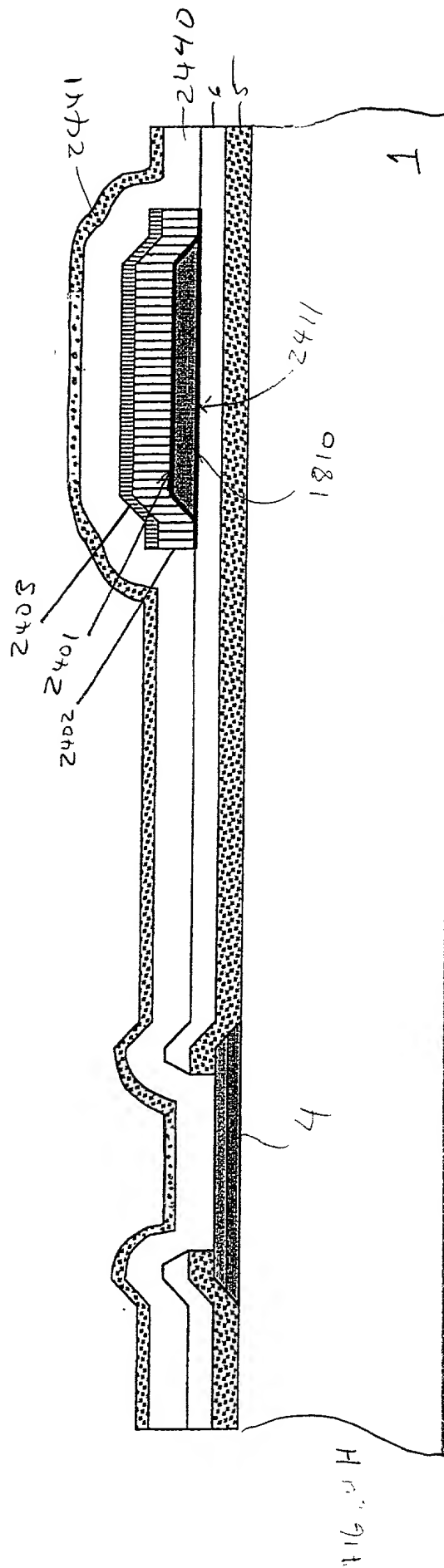


FIG. 24H

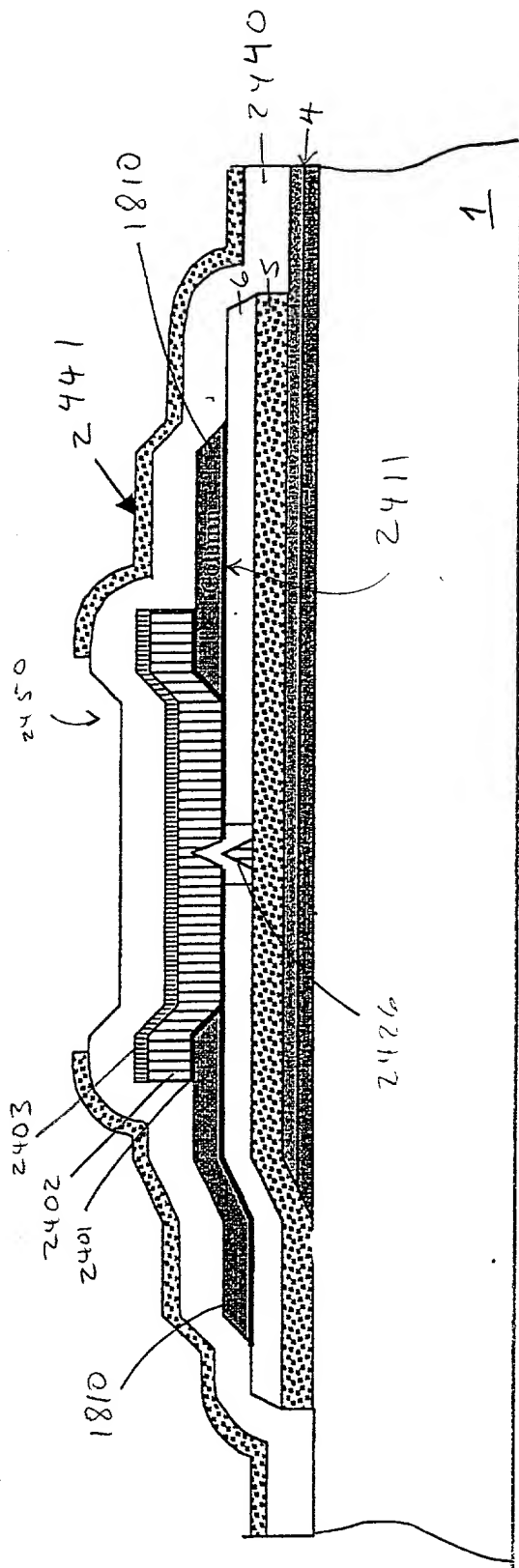


FIG. 24I

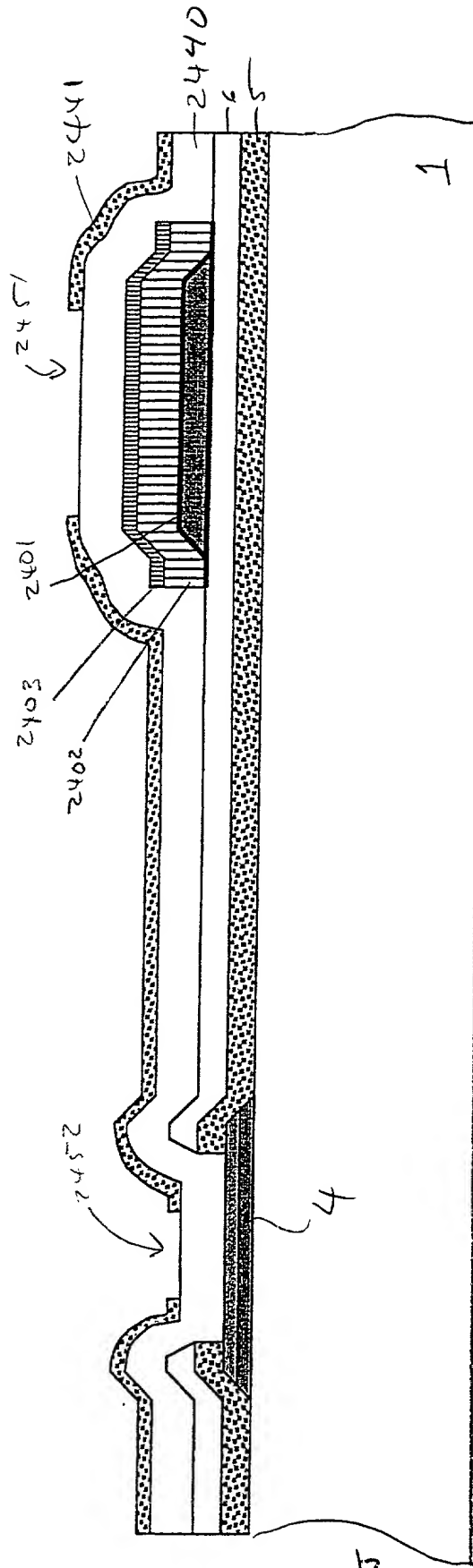


FIG. 24J

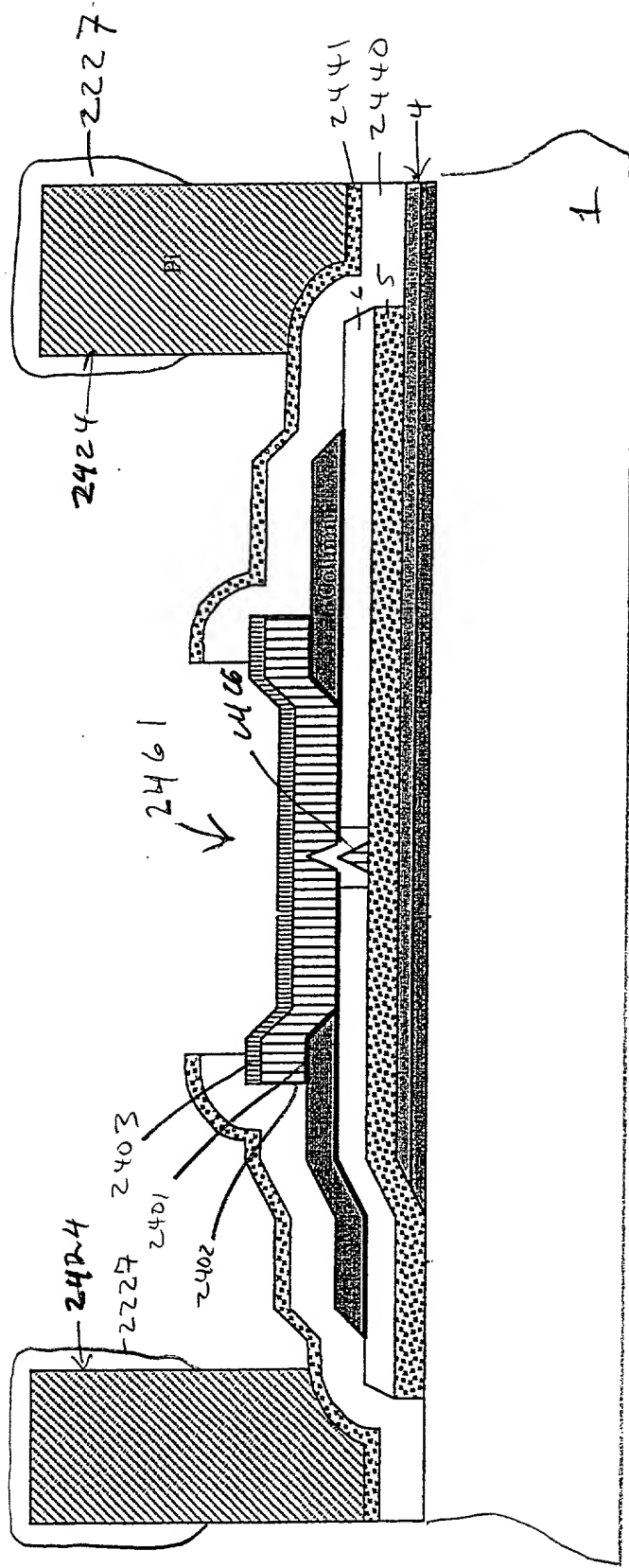


FIG. 24K

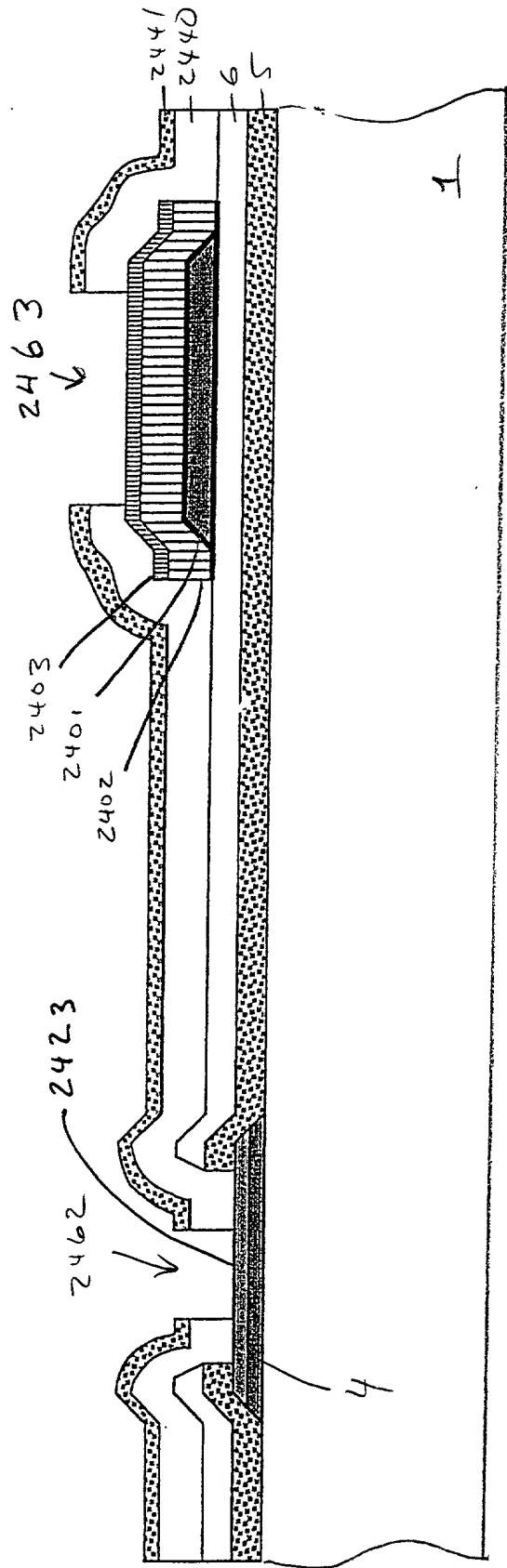


FIG. 24L

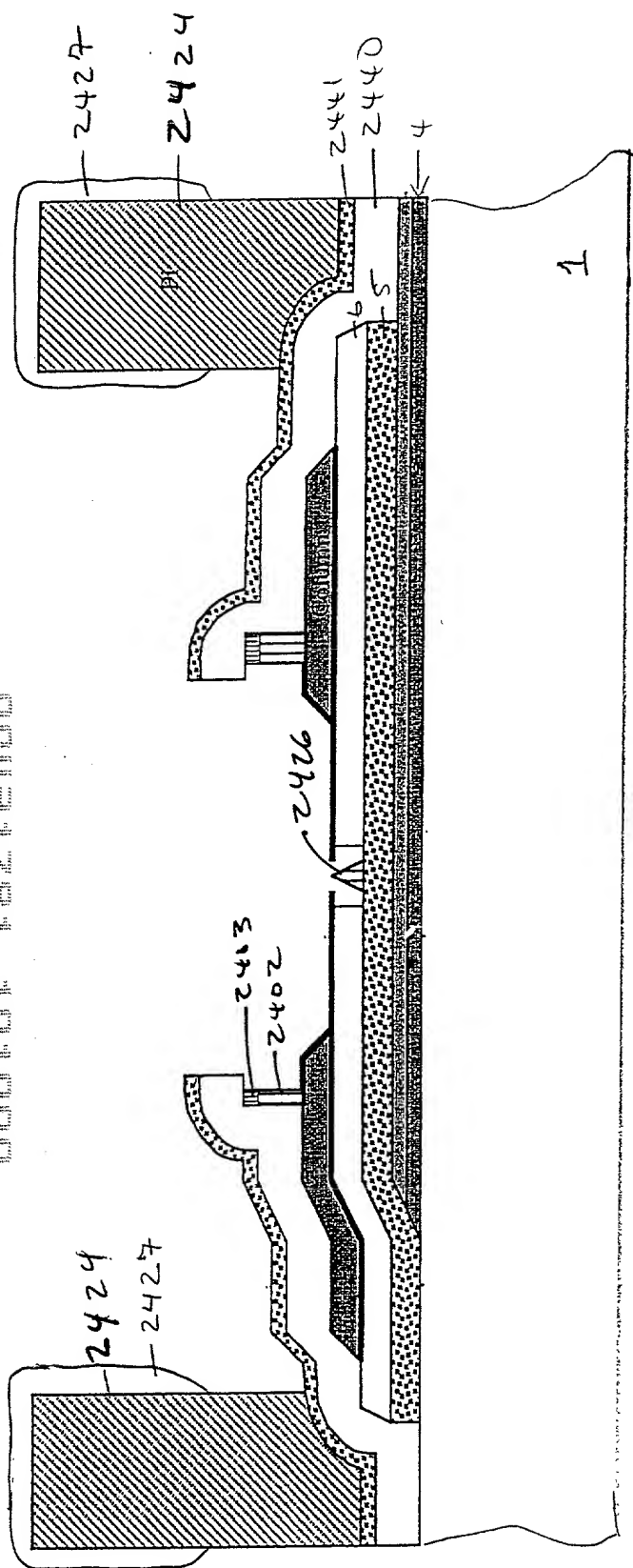
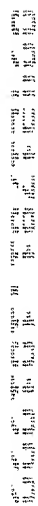


FIG. 24N

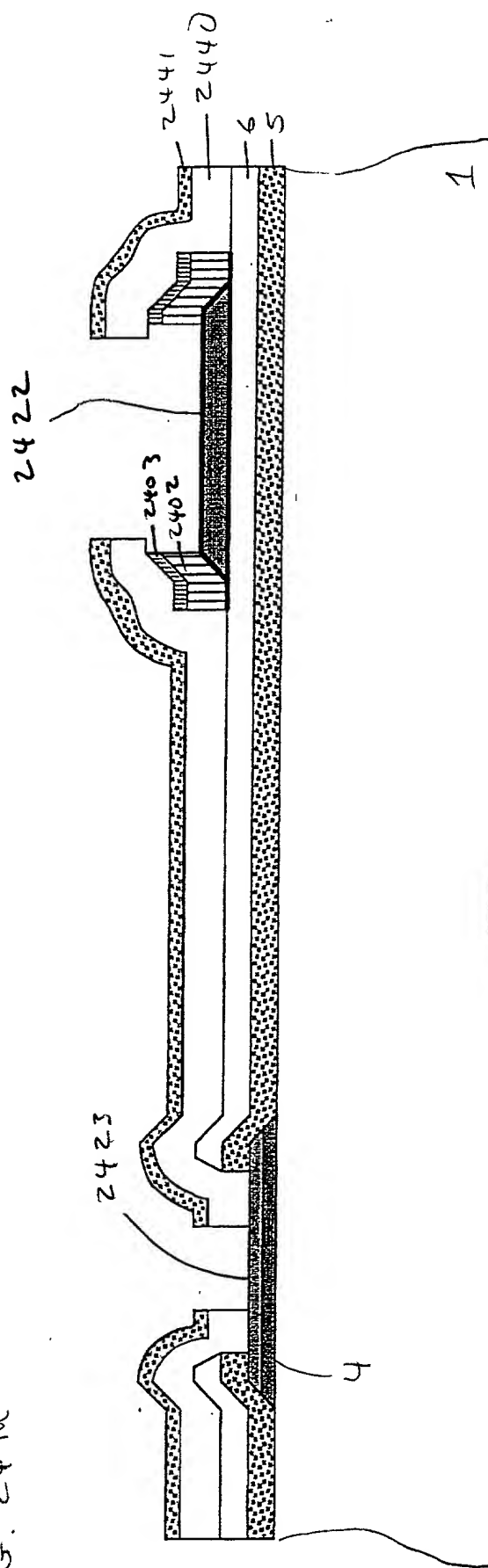


Fig. 24N

FIG. 25

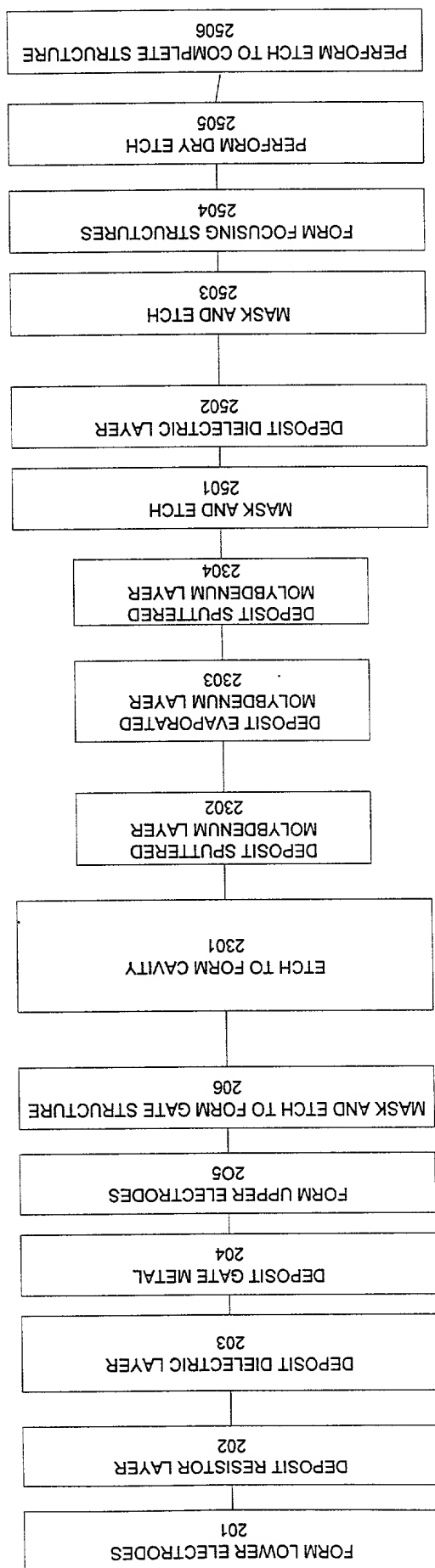
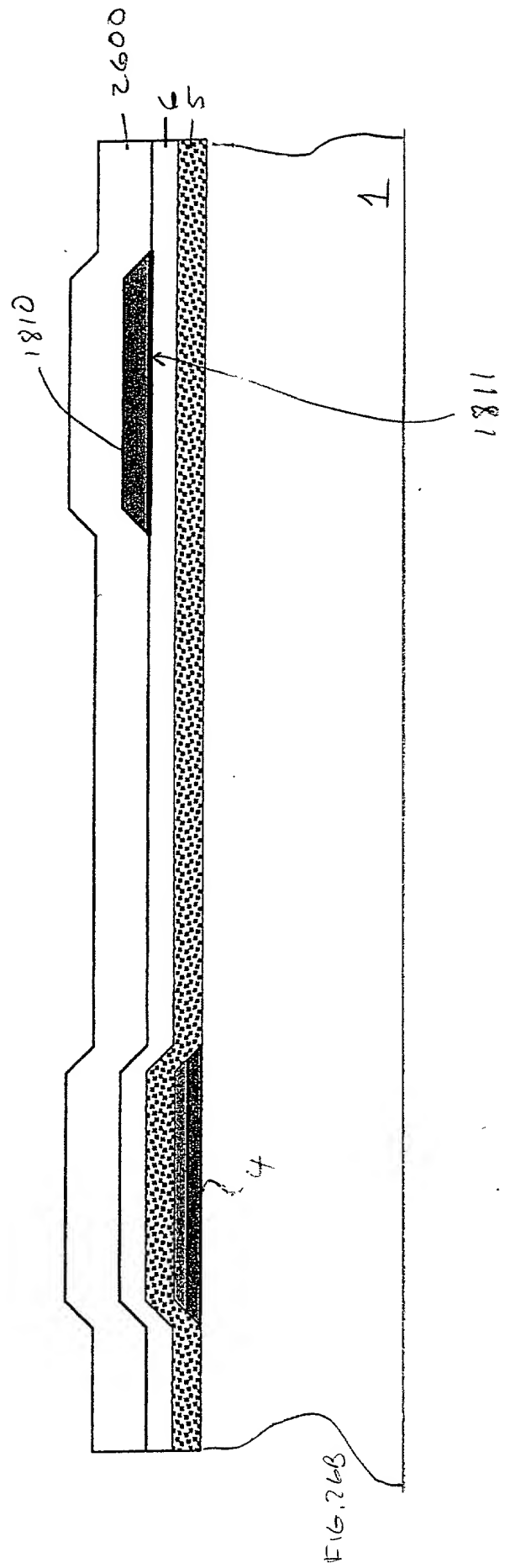
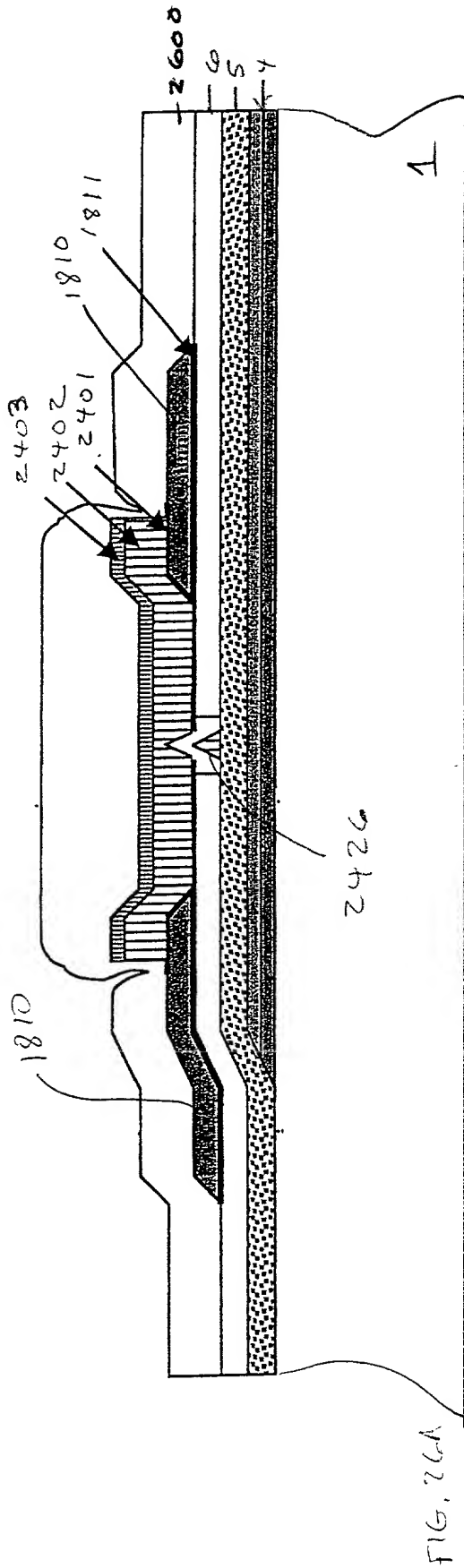
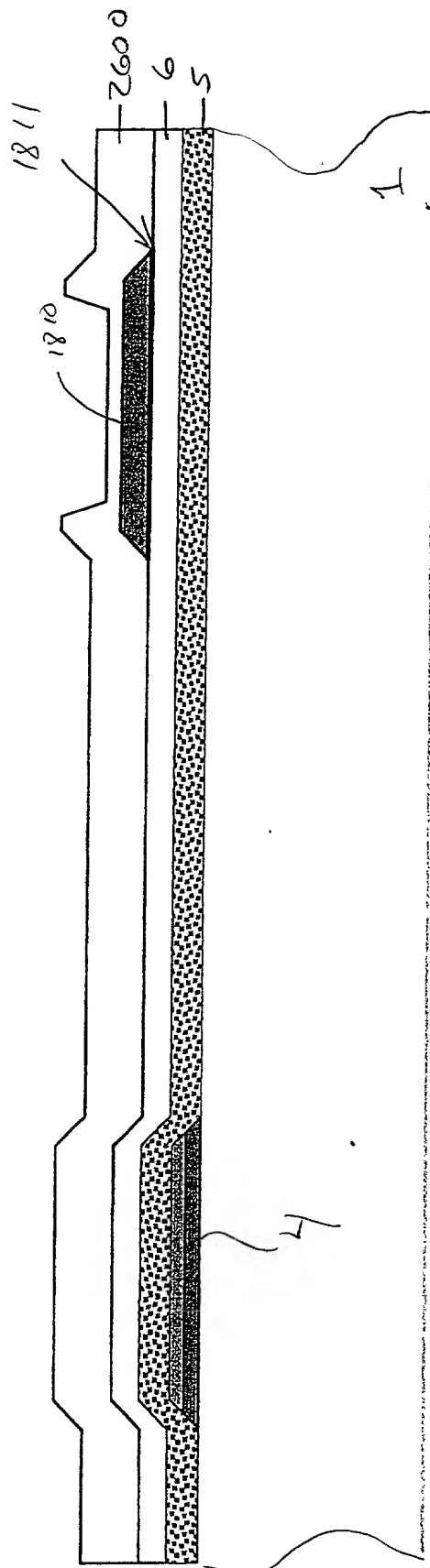
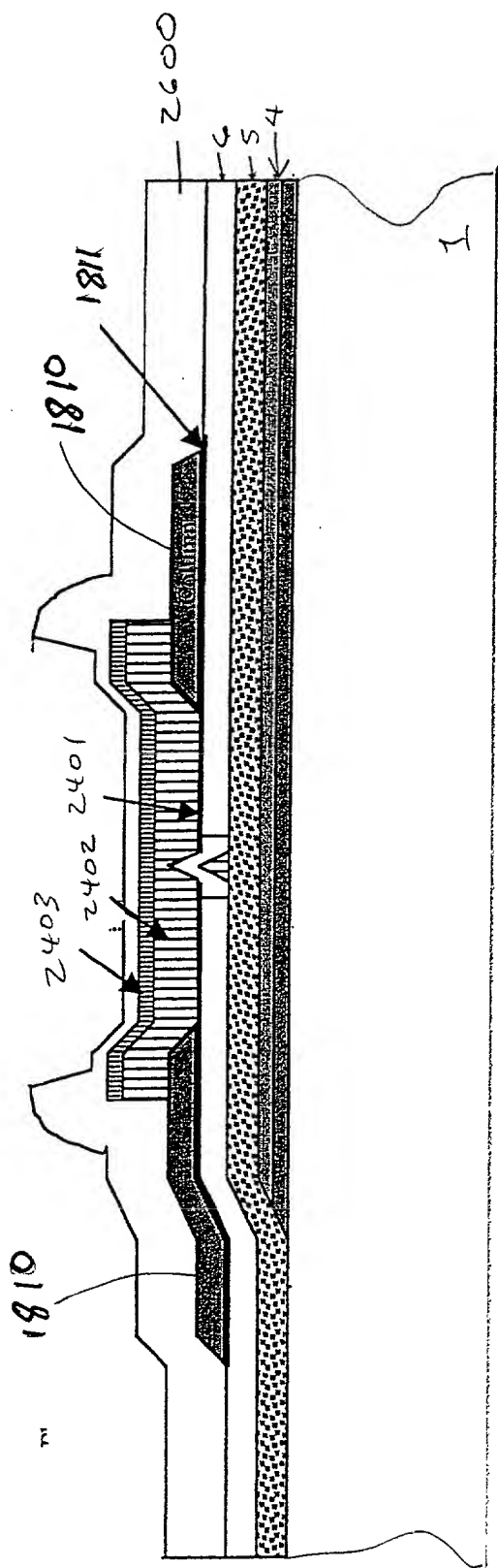
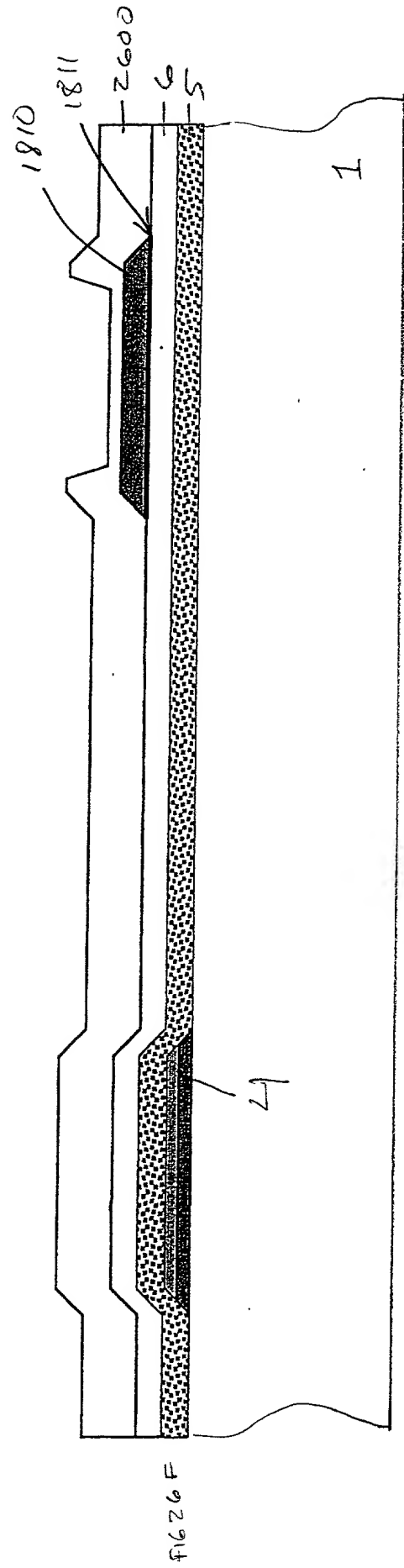
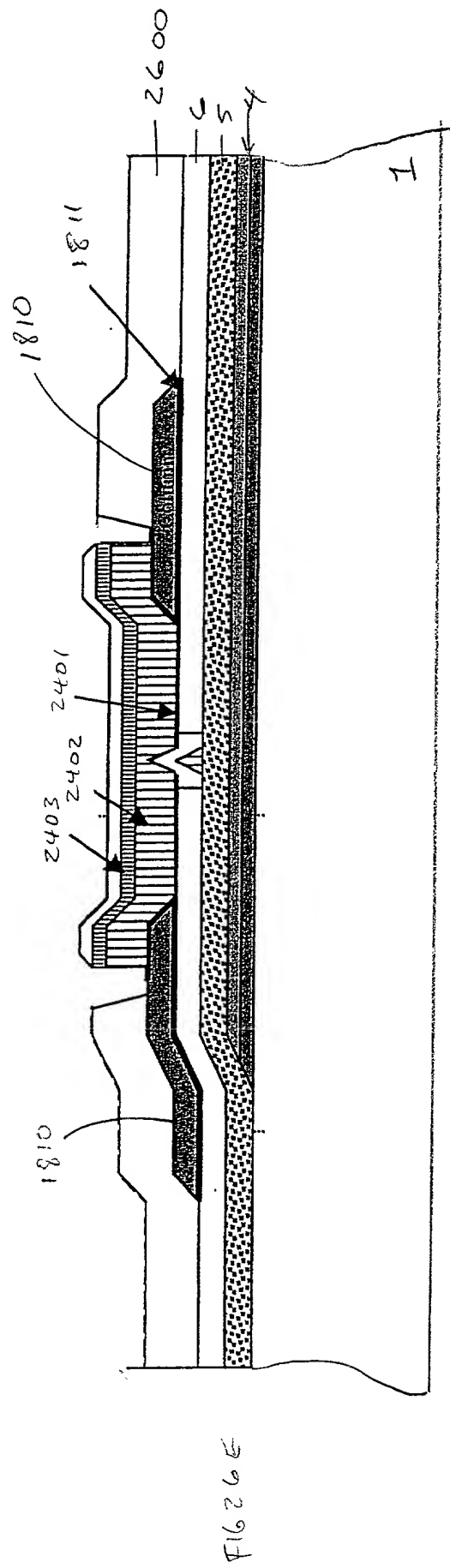
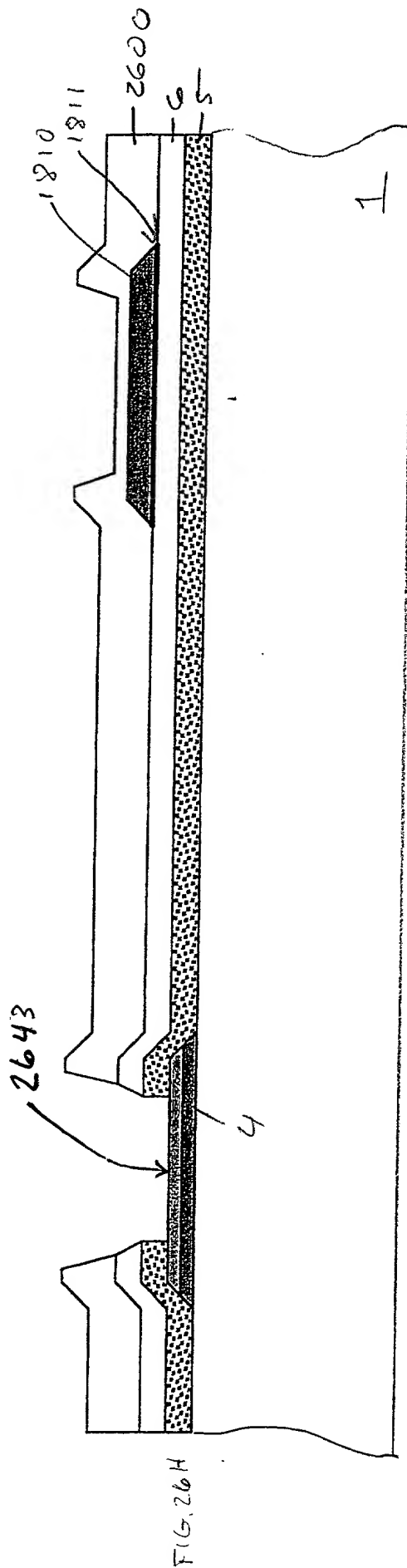
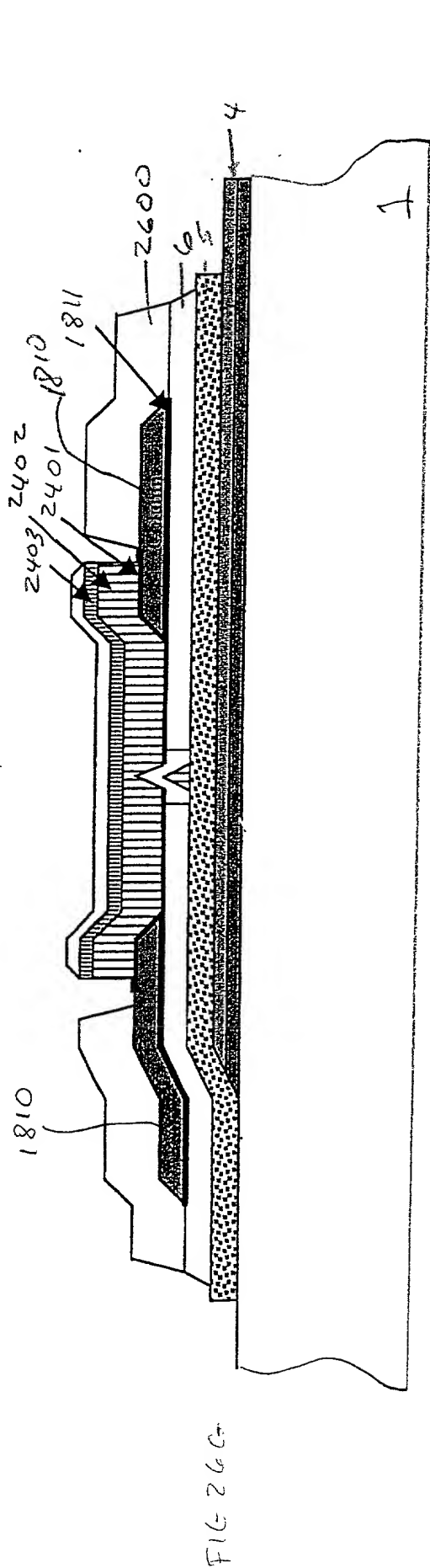


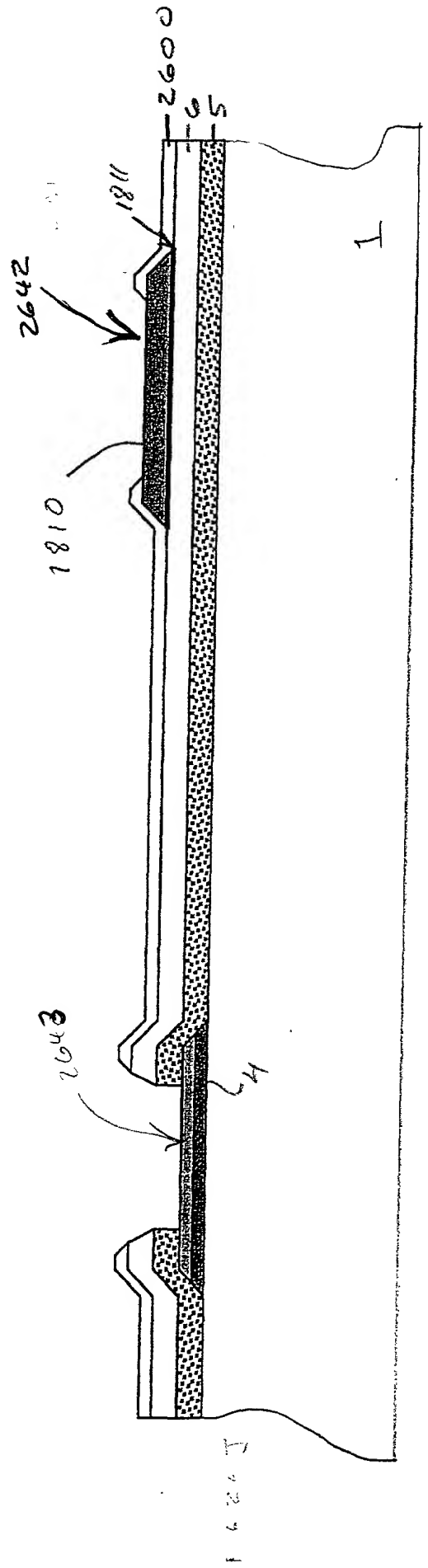
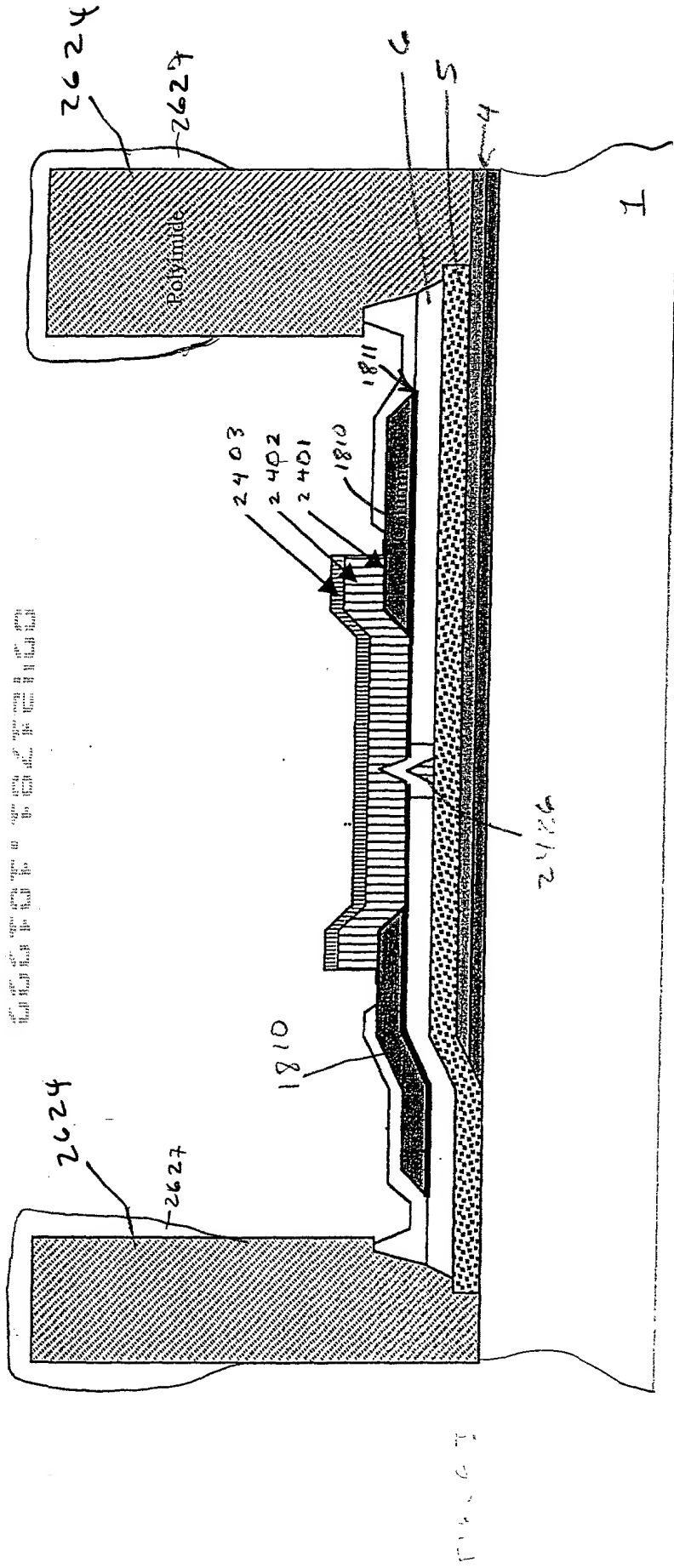
FIG. 25 is a flowchart of a semiconductor manufacturing process. The process starts with forming lower electrodes (201), followed by depositing a resistor layer (202), a dielectric layer (203), gate metal (204), and upper electrodes (205). A gate structure is formed by masking and etching (206). A cavity is then etched (2301), and three layers of molybdenum are deposited: sputtered (2302), evaporated (2303), and sputtered (2304). This is followed by masking and etching (2501), depositing a dielectric layer (2502), masking and etching (2503), forming focusing structures (2504), performing a dry etch (2505), and finally performing an etch to complete the structure (2506).











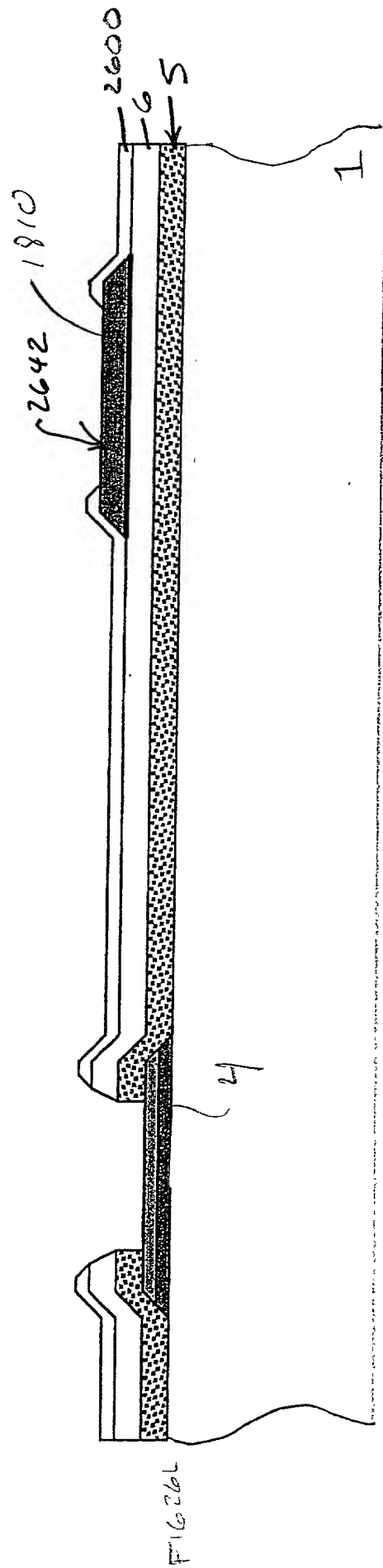
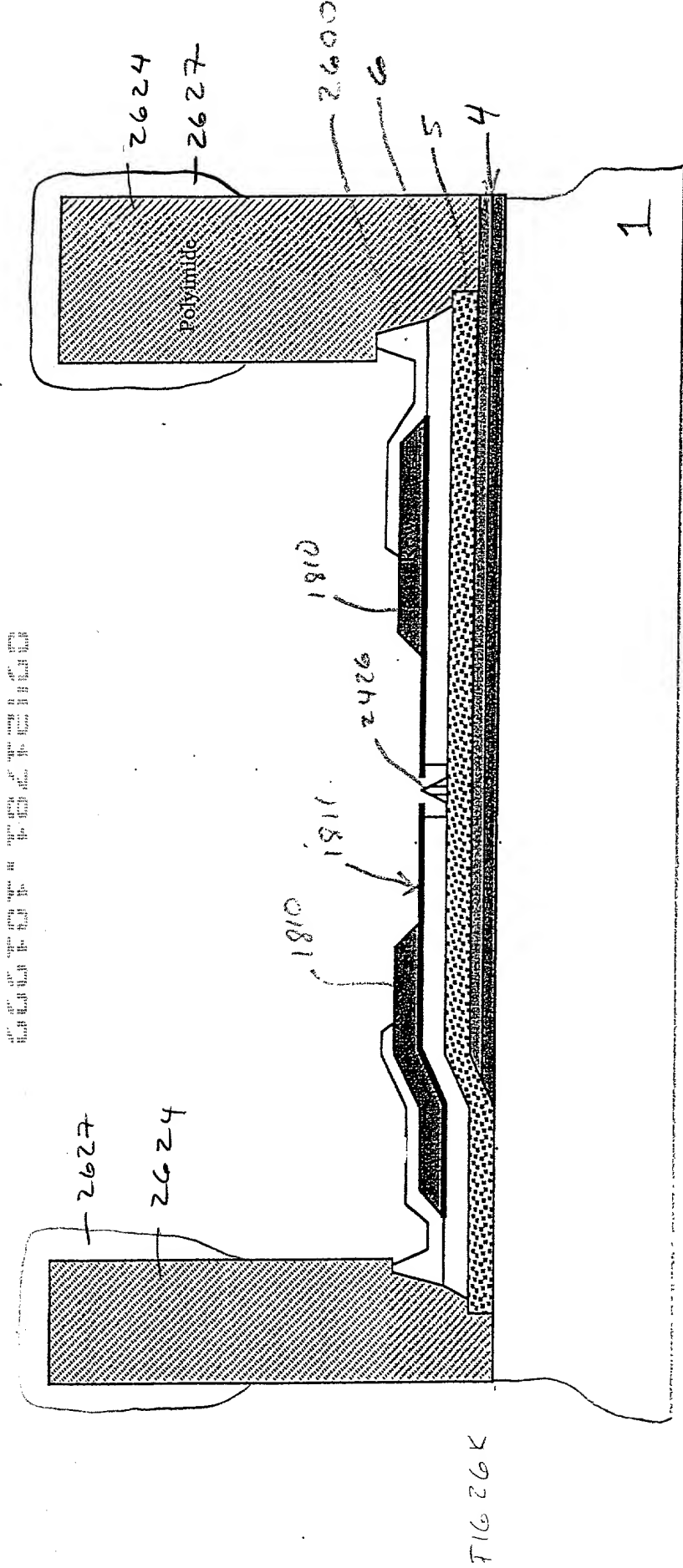
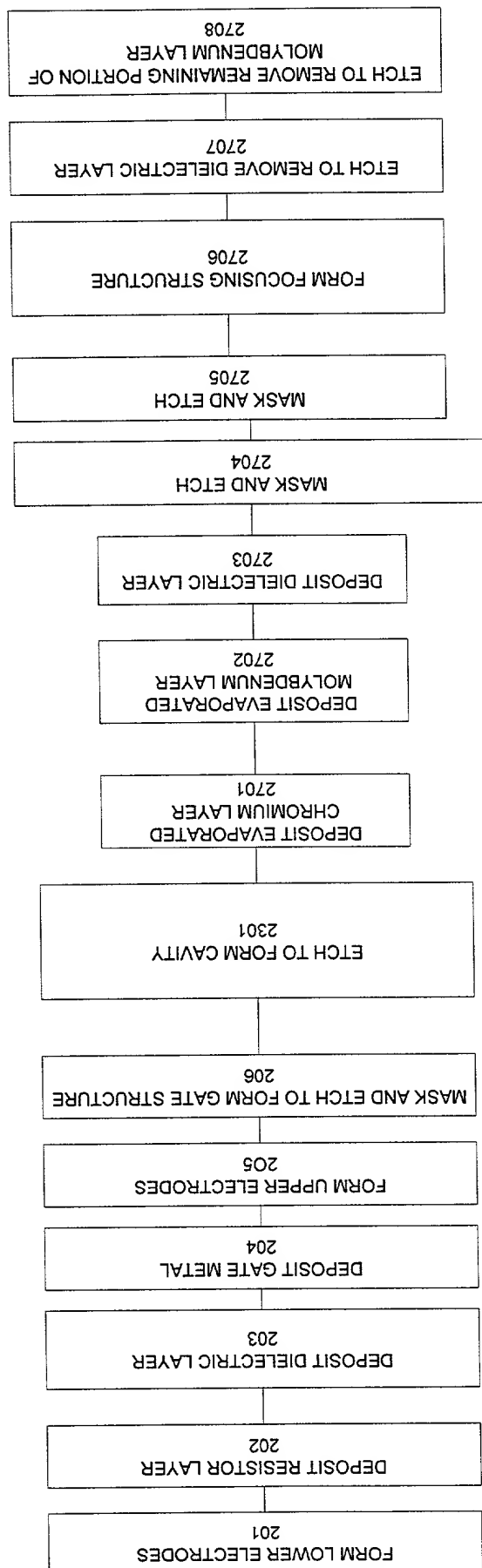
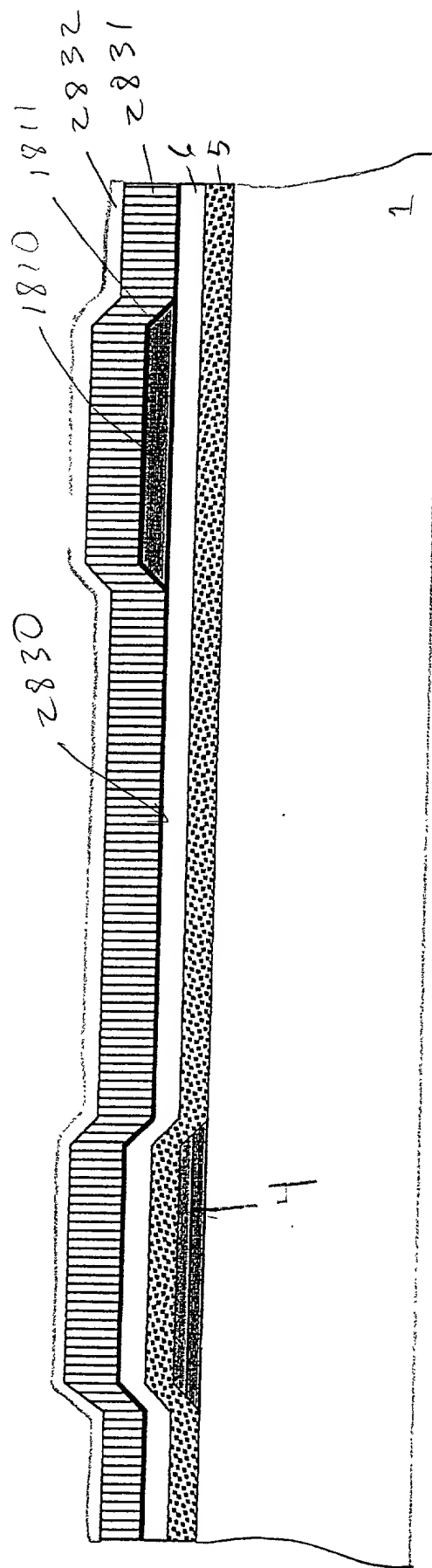
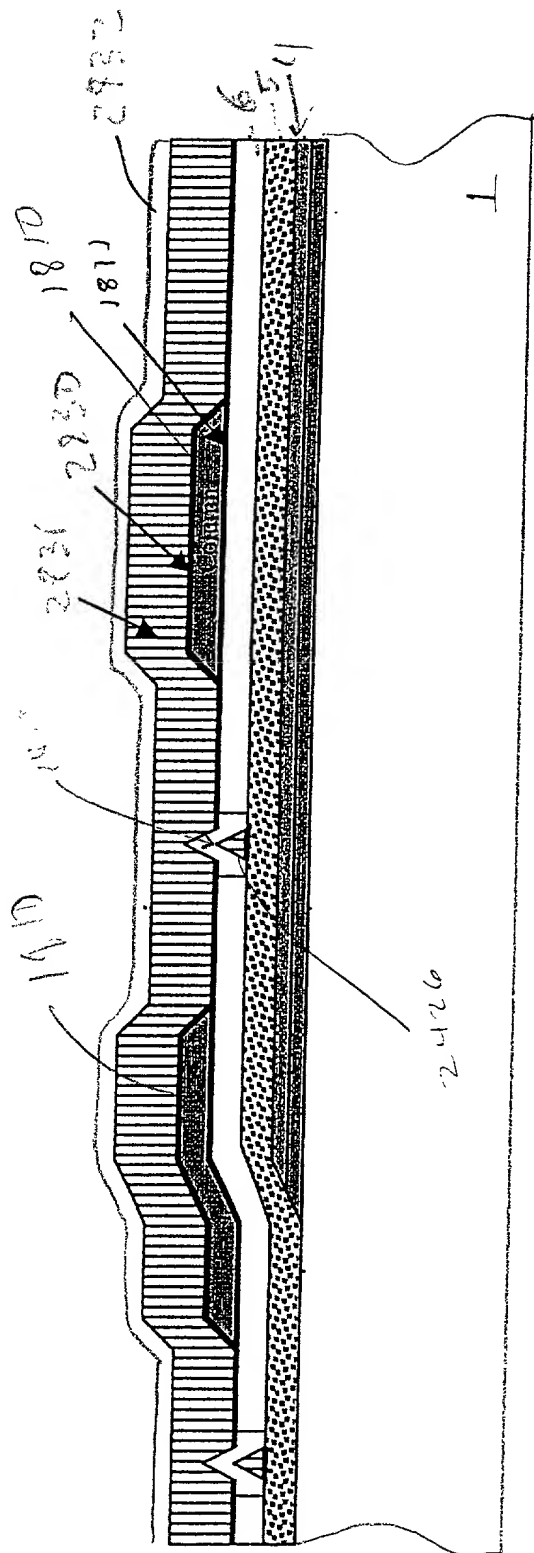


FIG. 27





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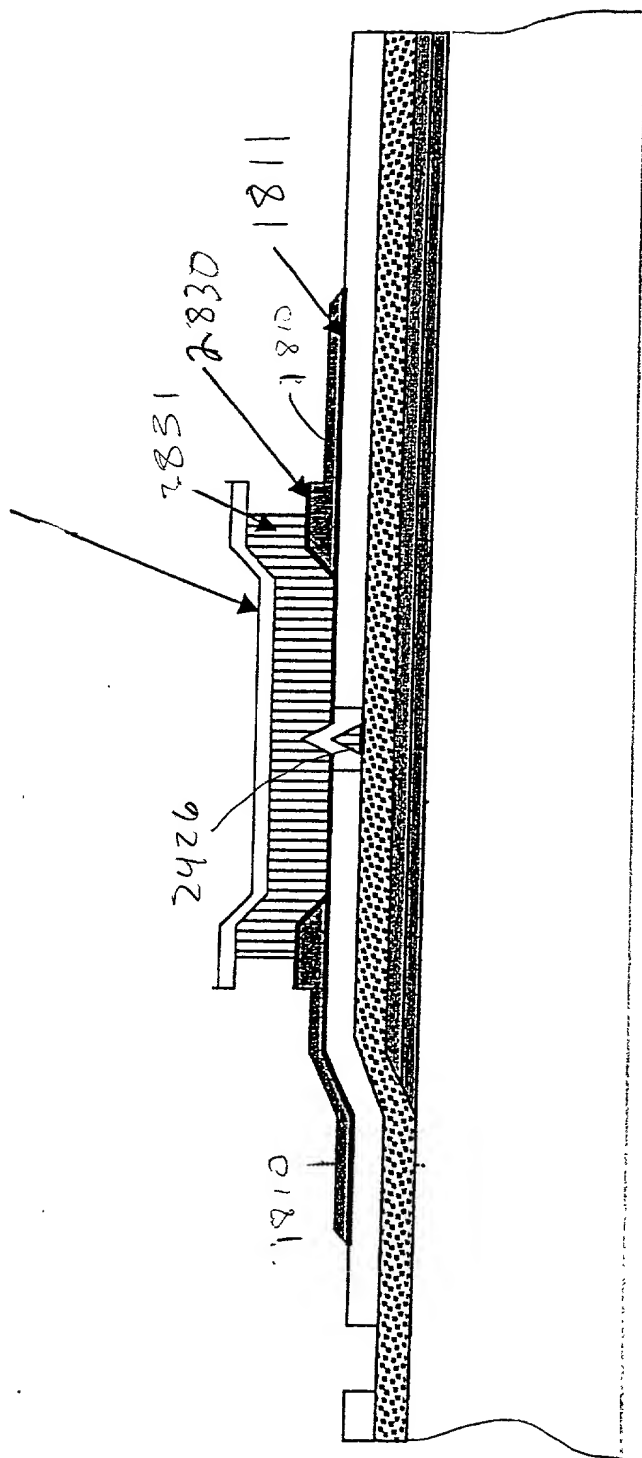


FIG. 28C

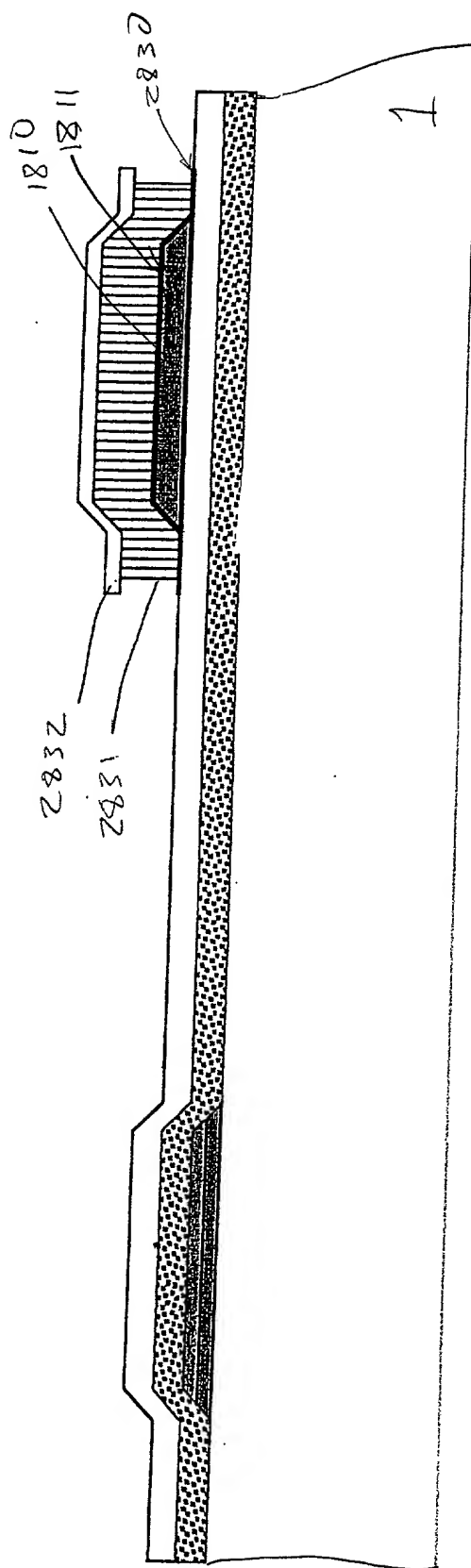
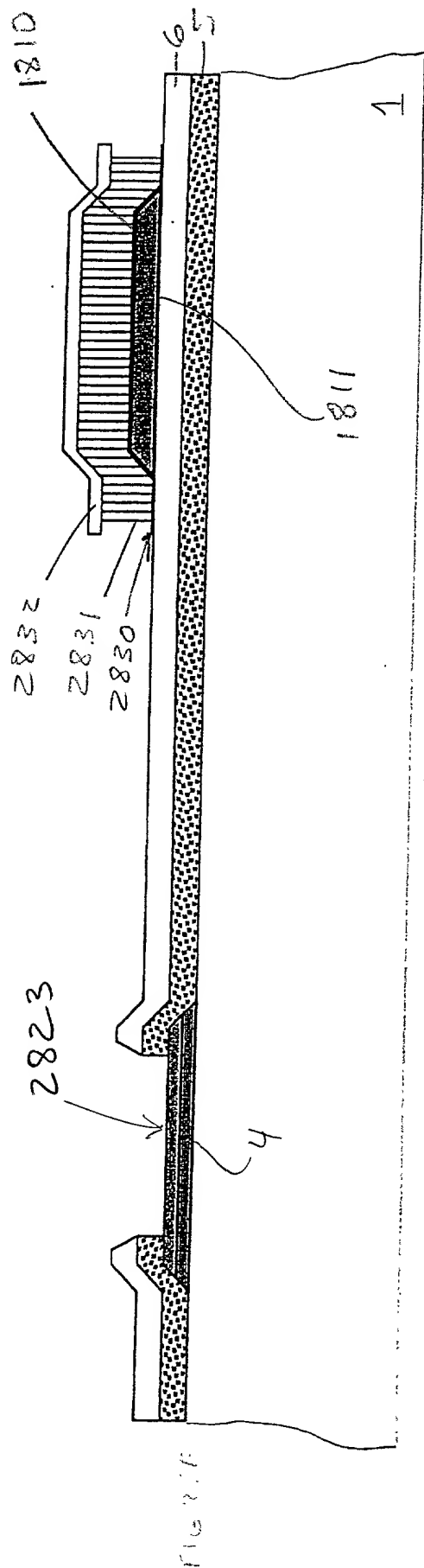
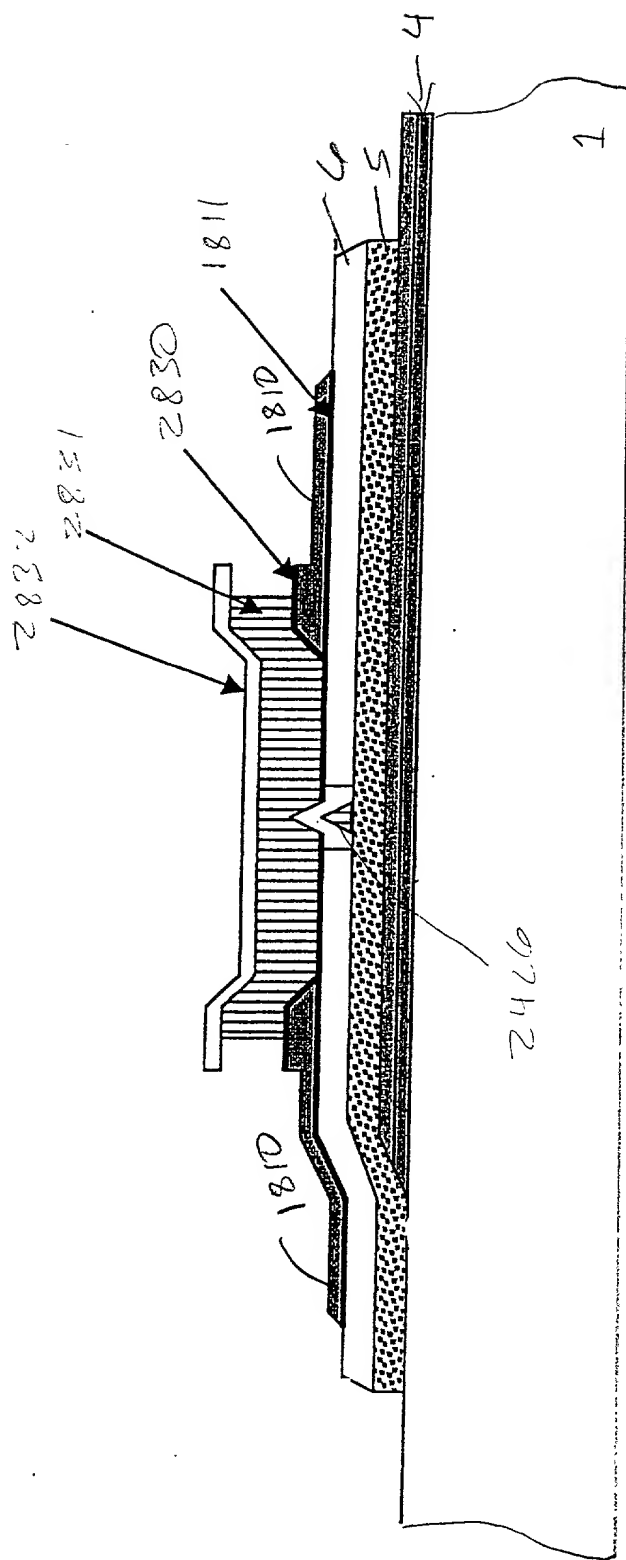


FIG. 28D



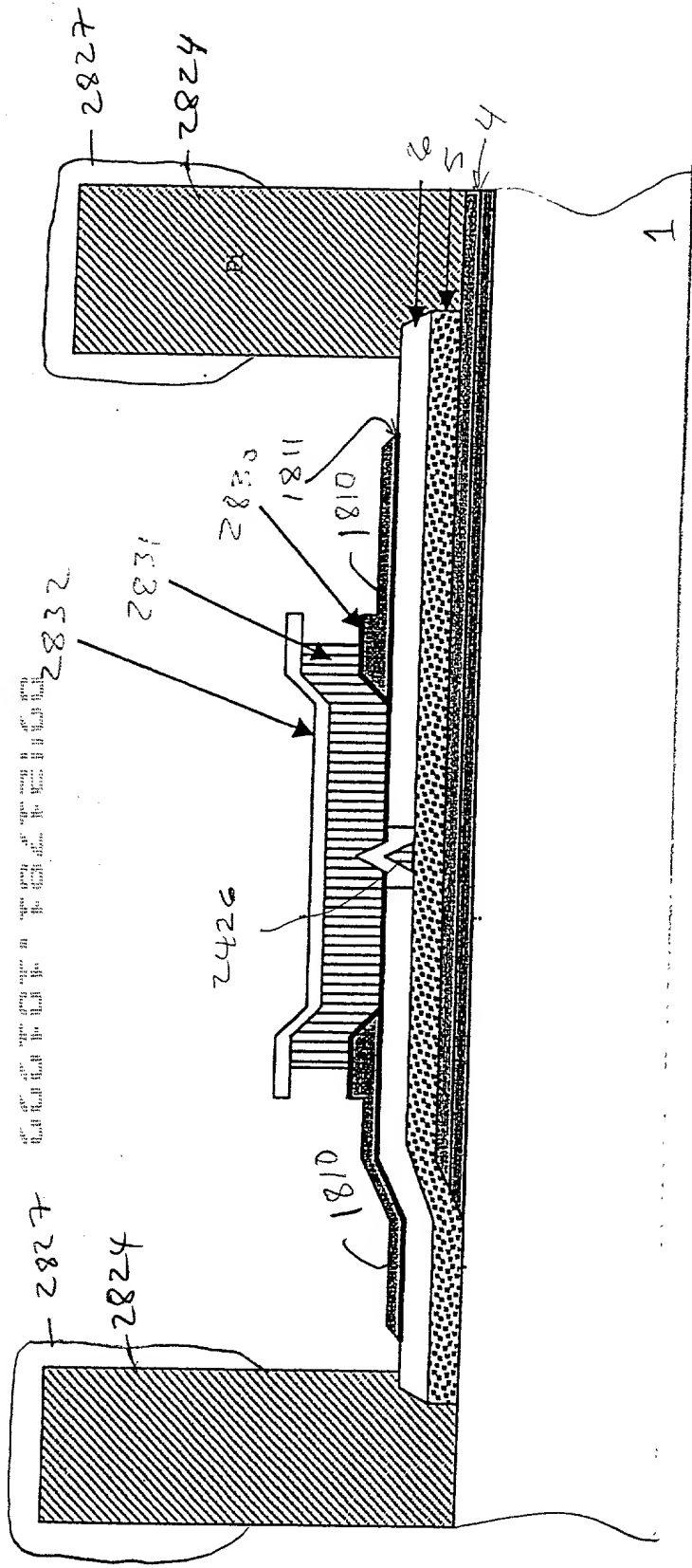


FIG. 28

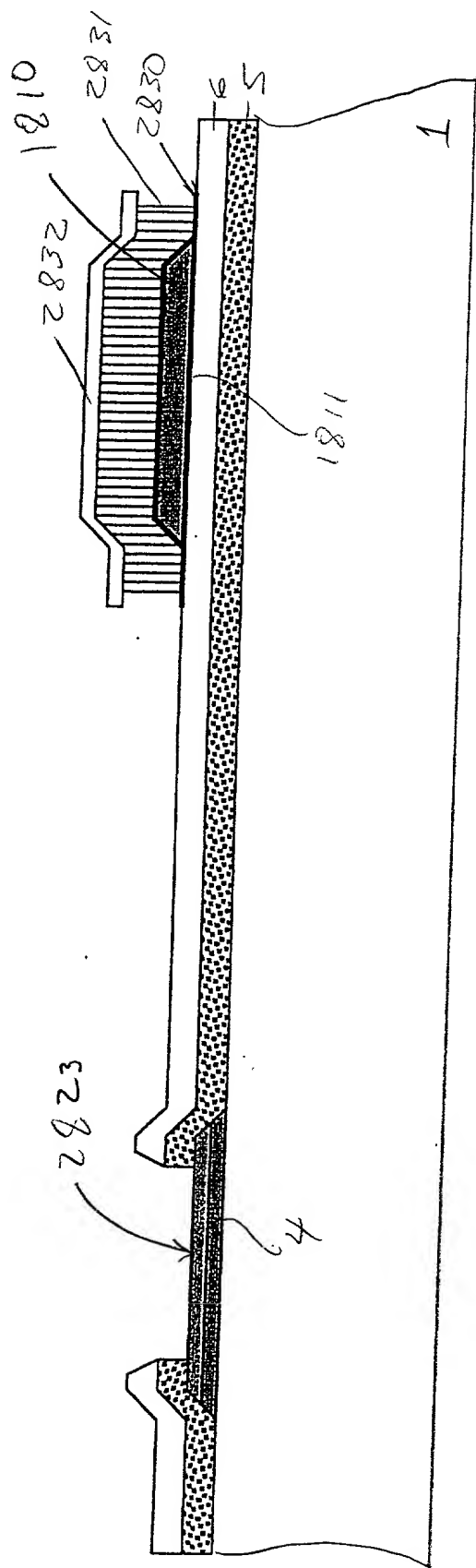
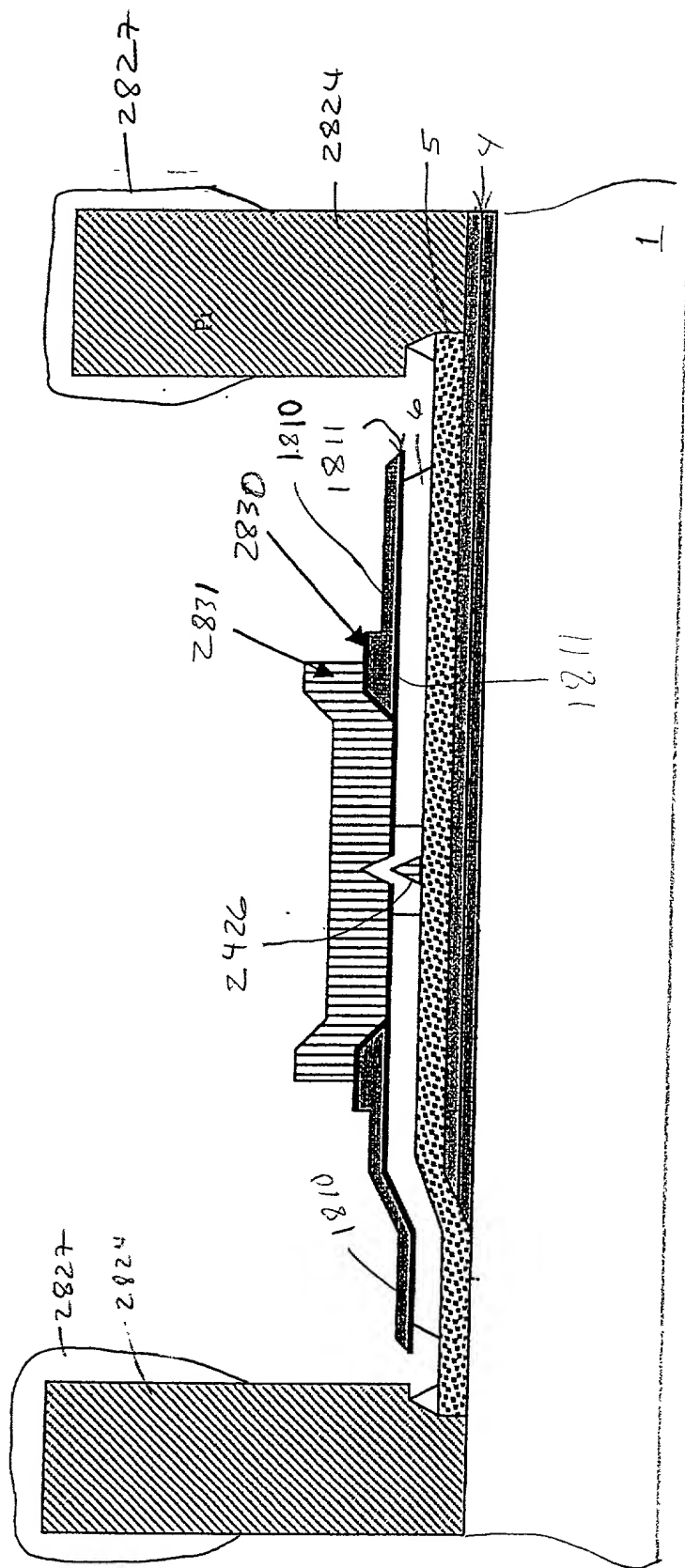
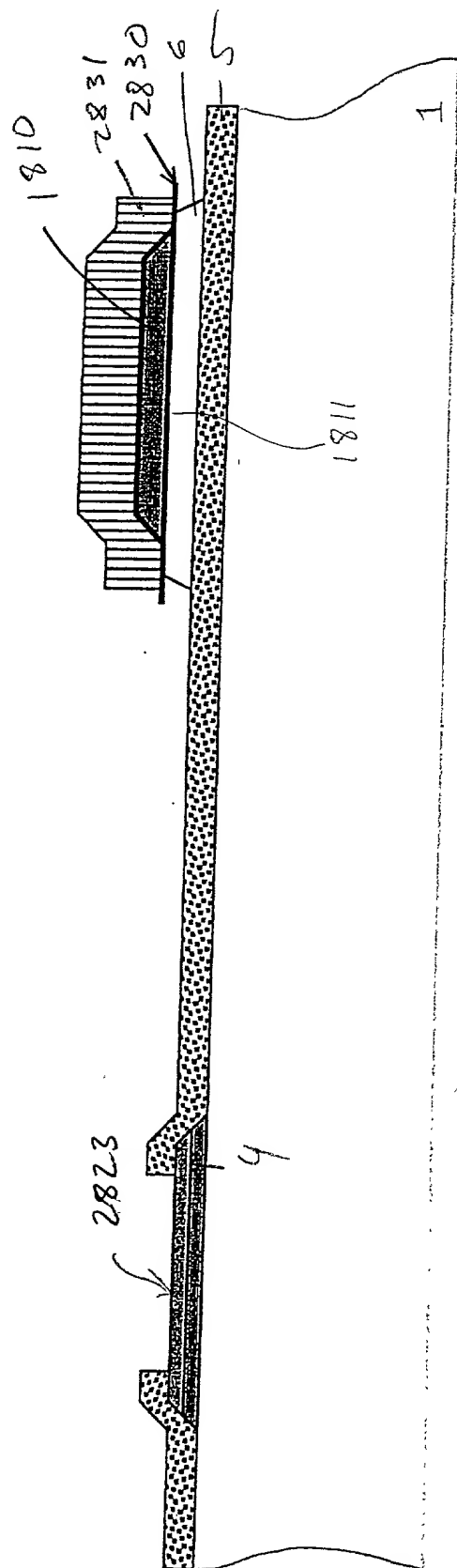


FIG. 29

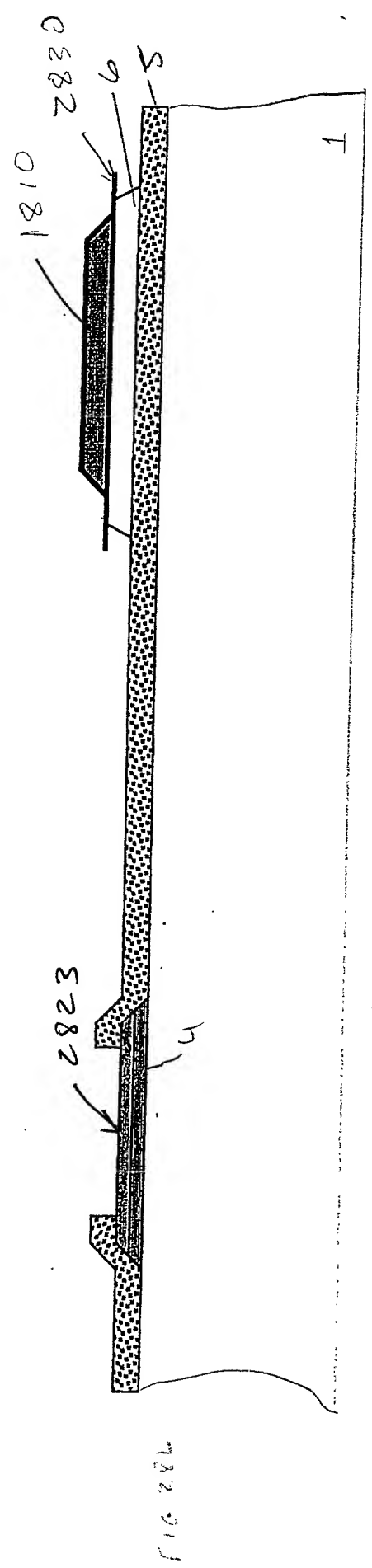
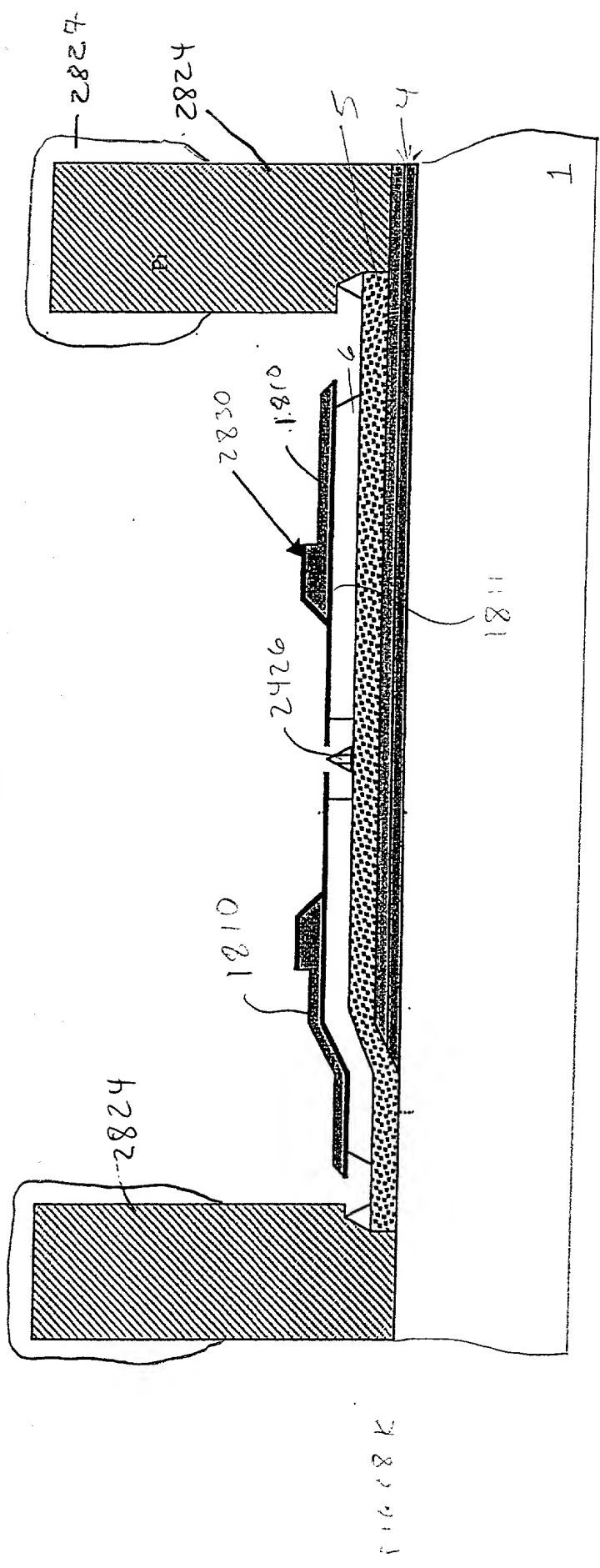


7-10-25



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FIG. 282



Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ELECTRODE STRUCTURE AND METHOD FOR FORMING ELECTRODE STRUCTURE FOR A FLAT
PANEL DISPLAY

the specification of which:

☒ is attached hereto, or
..... was filed on as application serial no. : and
..... was amended on

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed
.....	yes no
.....	yes no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
.....
.....

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

James P. Hao	Registration No.: 36,398
Anthony C. Murabito	Registration No.: 35,295
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Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature _____ Date _____
Residence _____ Citizenship _____
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(City State)

P.O. Address _____

Full Name of Fourth/Joint Inventor: **Matthew A. Bonn**

Inventor's Signature _____ Date _____

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P.O. Address

Full Name of Fifth/Joint Inventor: **Kishore K. Chakravorty**

Inventor's Signature _____ Date _____

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